ESD
APPLICATION HANDBOOK
AUTOMOTIVE EDITION

PROTECTION CONCEPTS, TESTING & SIMULATION FOR MODERN INTERFACES

Design Engineer's Guide

nexperia

ESD Application Handbook
Automotive Edition

Protection concepts, testing and simulation
for modern interfaces

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ESD Application Handbook — Automotive Edition
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for modern interfaces
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July 2020

www.nexperia.com

ISBN 978-0-9934854-5-9

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Preface

Nexperia is a leading expert in the high-volume production of essential semiconductors, components that are required by every electronic design in the world. The company's extensive portfolio includes diodes, bipolar transistors, ESD protection devices, MOSFETs, GaN FETs and analog & logic ICs. These products are recognized as benchmarks in efficiency – in process, size, power and performance — with industry-leading small packages that save valuable energy and space.

Our extensive portfolio of standard functions meets both the demands of today's state-of-the art applications and the stringent standards set by the automotive industry. Through our continued efforts in innovation, reliability and support, we maintain the leading position in all our key product segments. We develop and deliver benchmark solutions for today's and tomorrow's market requirements, drawing on a heritage of over 60 years' expertise in Semiconductors as the former Standard Product Divisions of Philips Semiconductors and NXP.

Our successful record in innovation is the result of varied yet streamlined R&D. We combine the latest technologies with efficient processes, helping us to serve the world's most demanding industries with world-class products.

Nexperia Design Engineer's Guides
Our program of Design Engineer's Guides has one key goal: We want to share our Expertise with you and help you to optimize your electronic designs. It is a collection of technical and application insights, "from Engineer to Engineer".

The first Nexperia Design Engineers Guide, released in 2017, is our *MOSFET Application Handbook* [1]. In this handbook, our engineers focus on how to use MOSFETs in specific applications and what the key and critical MOSFET parameters are, considering aspects like thermal conditions etc.

The Second Technical Guide of this series was launched in 2018: Our *ESD Application Handbook* [2]. We focus on Protection Concepts, Testing and Simulation for Modern Interfaces. Nexperia got a lot of positive feedback from our Engineering Community, from our Customers representing all Industries word wide. In addition to this ESD Application Handbook, Nexperia is also offering on-site Technical ESD Seminars to share our insights with our customers, cross all relevant applications like Automotive, Mobile Communication, Consumer, Computing and Industrial. At the end we want to help minimize the risk of ESD damage — supporting the design community in protecting applications and products against ESD issues. Both Design Engineer's Guides are also available in Chinese Version [3], [4].

Clearly in the last decade the Automotive industry has been changing faster than ever, a trend that shows no sign of stopping. Electrification and Autonomous Driving are already being implemented or on the way, while 5G will enable Car-to-X communication, intelligent traffic management, etc. The innovation rate is much faster than in the previous decades.

However, ever increasing vehicle electrification and connectivity leads to an increase in the amount of data which needs to be transferred in the car. High ESD robustness is key to ensuring the reliable, high performance demanded by automotive applications. The challenge hardware engineers face is that as data rates increase, ESD robustness decreases.

So, to address the dynamic and demanding challenges faced by the Automotive industry we decided to publish a special edition of our *ESD Application Handbook*:

Nexperia "ESD Application Handbook — Automotive Edition"
This Handbook will give you an introduction into ESD (Electro Static Discharge) basics including an overview of ESD protection principles, ESD testing standards and TLP (Transmission Line Pulse) testing, Key Datasheet Parameters and how to interpret these.

Next to classical In-Vehicle Networks you will also get some insights about Ethernet and other interfaces in modern automotive applications like HDMI, USB and MIPI. And at the end we round up the Automotive Edition with some background information about modelling ESD events.

Please take now some time to study our *ESD Application Handbook — Automotive Edition*. The Table of Contents make it easy for you to navigate to the key chapters of interest. This book is another key milestone to build the Technical Nexperia Encyclopedia.

Finally, I want to thank Dr. Jan Preibisch, who has significantly contributed to this special edition.

Olaf Vogt
Director Application Marketing
Nexperia

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Chapter 1

Introduction

Three major trends are shaping the automotive industry of today and tomorrow: electrification, autonomous driving and connectivity. Electrification is pushing us towards less electrical control units (ECUs) because an electric drive needs less control modules. However autonomous driving and connectivity are driving ever increasing data rates in vehicles and the number of communication nodes driven by these two trends is set to explode. Especially with the rapidly increasing number of sensors, like cameras, radar, and lidars. Data rates are also increasing, as there is more and more data to transmit.

Today's challenge for development engineers in the automotive sector is to keep up with all these trends, make them work in the harsh automotive environment , and provide the expected high quality. External electrostatic discharge (ESD) protection devices are an essential tool used to keep up with the requirements that are getting tougher. While these devices are often used "off-the-shelf", the characterization of the devices and their interplay with the surrounding system can be more complicated than anticipated at first sight. This handbook aims to provide technical background and practical insights to assess external ESD protection with respect to the target application and choose the right product to achieve high system level robustness against ESD and voltage surges while maintaining signal integrity and electromagnetic compatibility (EMC) compliance.

1.1 Automotive trends

Out of all the trends in automotive, autonomous driving and connectivity are most relevant in the context of ESD protection. The term autonomous driving has been hyped over the last few years and some observers are already disappointed by the false promises of self-driving cars being on the street within one decade. Even though fully autonomous cars remain more of a dream due to technical but also regulatory reasons, partial and conditional automation is already a reality. The latest versions of luxury cars offer features that allow us to drive on the highway or in a traffic jam without human interaction. And self-parking cars have been around for a few years. These advanced assistance systems as well as others all come under the term, Advanced Driver Assistance Systems (ADAS).

On a hardware level these systems have exceptional reliability requirements and often operate with multiple redundancy levels. They generate massive amounts of data which need to be transmitted throughout the car. And as these systems tend to be "real-time" capable, latency must be low and link errors cannot be tolerated. In terms of ESD, the interfaces are required to be very robust in general, tolerant against ESD during operation (powered ESD) preventing link errors, and support the highest data rates. In fact today's automotive interfaces reach speeds (up to 15 Gbps) that are comparable with or even better than modern consumer interfaces.

Connectivity is a diverse term referring to many possible interactions of the car with the driver's electronic equipment, roadside infrastructure, other vehicles or electronic devices. Seamless integration with the Internet of Things (IoT) and cars talking to each other to improve overall safety, are just two sub goals. Supporting technologies for the enhancement of connectivity include wireless (5G, WiFi, and NFC) and wired (USB 3.x and HDMI) standards. There are still competing technologies when it comes to vehicle to anything (V2X) communication, standards in preparation and in most regions of the world the mandatory telematic box (T-Box) is pushing the industry. Clearly, robustness requirements are not as high as for ADAS, as safeguarding human life is not directly dependent on the operation of these systems. However, as the environment of the car is generally harsh from an ESD perspective and given the cost of replacement and customers quality expectations are usually high, interfaces are usually designed to be as robust as possible.

1.2 Trends in IC technology

Shrinking silicon geometries allow more complex electronic content to be squeezed into small spaces. With these new silicon processes, oxide layers have become thinner and the gates of embedded FETs are therefore more vulnerable to surge events. High voltage events of up to 30 kV peak voltage with about 100 ns overall pulse width that result from ESD must be considered. As do surge events with a longer pulse width of about 60 µs and less extreme voltage levels. In general designers can no longer rely on the internal ESD protection structures of the system chips. Internal ESD protection is sufficient to protect components during the assembly process in a relatively ESD safe environment. However, it does not protect against ESD events seen in the field. External protection therefore cannot be viewed as a luxury or left out.

Modern high-speed and super-speed interfaces operate with reduced signal levels. High data speed, up to 20 Gbit/s, requires a carefully designed printed circuit board (PCB) layout to maintain signal integrity. This can be achieved by proper impedance matching, avoiding unacceptable losses and reflections. Additionally, various EMC aspects must be considered in a vehicle. From a compliance perspective, ESD is just one aspect of EMC. Especially important for consumer and ADAS interfaces, it is increasingly true for traditional automotive interfaces as the trend of less robust system basis chips (SBC) that integrate CAN or LIN transceivers is more common. Hence, external ESD protection devices are always of relevance and will not become superfluous with more modern integrated circuit (IC) technologies. Rather, the opposite is the case.

1.3 Trends in ESD protection technology

Historically, the technology of ESD protection devices has advanced with the increasing data rates of the interfaces and the decreasing robustness of ICs. At first capacitors where used but because of the limited effect on ESD, and non-applicability on data lines, todays design methodologies do not rely on capacitors anymore.

The standard technology of ESD protection is a Zener diode-based design. They are very reliable, and can be very robust themselves, however the clamping voltage is by design rather high and thus, in many cases, the protection is not good enough for a sensitive IC. Furthermore, the parasitic capacitance is too high for their application on high-speed data lines. Rail-to-rail technology uses pn-diodes to hide the capacitance of the Zener diode, allowing the application of Zener technology to high-speed interfaces. However, the clamping behavior is even worse than for the Zener diode alone.

Varistors can have low capacitances but a much poorer clamping behavior compared to a silicon-based solution. Additionally, repetitive ESD events can deteriorate the devices leading to significantly increased leakage currents and change the parasitic capacitance value. Thus, varistors are not the first choice in protection of automotive interfaces.

Modern protection devices for high-speed automotive interfaces are based on advanced silicon structures, including silicon-controlled rectifiers (SCRs) and open-base technology. These advanced technologies allow a significantly improved ratio of the device robustness and the parasitic capacitance. The parasitic capacitance of cutting-edge protection devices is so low, that the parasitics of the

package dominate the RF characteristics. Additionally, these technologies allow for extremely low clamping voltages providing the highest system level robustness. Snap-back devices allow clamping voltages that are even below the trigger voltage.

Regardless of the application or interface, when choosing an ESD protection strategy, there are three essential parameters. The first is a high robustness of the protection device itself against ESD and surge events. The next is a low clamping voltage with a low dynamic resistance. A low dynamic resistance stands for a steep I-V-curve of the protection, so that clamping voltage does not increase much if surge current is increased. These requirements are extremely important to achieve a high system level robustness — the primary goal of why ESD and surge protection is applied.

Figure 1 shows the three key parameters of ESD protection devices and the performance of different technologies. Under the name TrEOS Protection Nexperia offers an ESD protection technology that combines benchmark values for all three key parameters — deep snap-back, low dynamic resistance and high ESD robustness with very low capacitance. This technology is ideally suited for super-speed data lines such as RX/TX lines of USB 3.2 or Thunderbolt interfaces, to protect very sensitive systems on chip (SoCs), and is also available in an automotive qualified version.

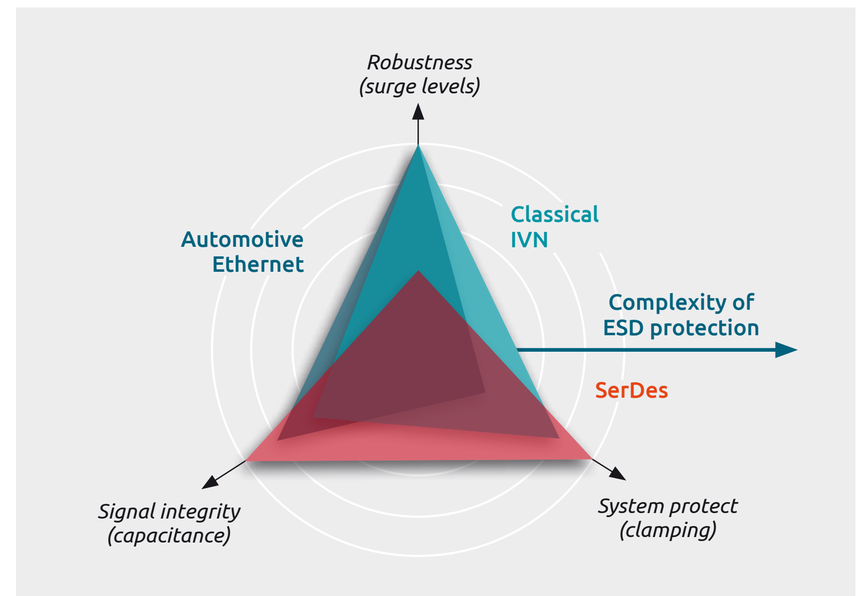


Figure 1 | Challenges of ESD protection and performance of different technologies

1.4 On the structure of this Handbook

First, this handbook provides an overview of ESD protection in automotive systems. Key parameters found in datasheets are explained in detail and how to choose a suitable component for a design based on this information. Various testing standards have been established to allow reproducible testing and qualification of electronic components and products. The most important testing methods are discussed in this handbook and how to use the 'new' Transmission-line pulse (TLP) testing method. It introduces a scientific selection process for ESD protection devices, overcoming the time-consuming trial and error testing that does not necessarily find the best solution. Furthermore, different ESD protection technologies and concepts are compared providing practical insights.

Information about the physical layers for automotive interfaces is presented and grouped according to different topologies used in today's cars. Starting with classical in-vehicle networks (IVN) like LIN and CAN, the Handbook proceeds with automotive Ethernet, the core of the up-to-date zonal architecture. High speed Serializer/Deserializer (SerDes) interfaces and multimedia interfaces complete the picture. These layer specifications are relevant for the selection of adequate ESD protection, to maintain signal integrity, and to choose the most suitable ESD diode topology respecting signal levels and the structure of drivers and receivers. Finally, the topic of supply line protection against high-energetic surge pulses is addressed.

In the last Chapter of the handbook, the so-called System Efficient ESD Design (SEED) methodology to simulate ESD events is introduced. This methodology models the behavior of ESD protection devices and system chip interfaces as individual blocks as well as in combination, to judge if the two components fit together and are safe against ESD and surge events.

Chapter 2

Datasheet parameters of ESD protection devices

To select suitable ESD protection devices, development engineers have to compare key parameters that can be found in vendor datasheets. In this chapter the most important key parameters and their relevance for a well operating interface are described. Furthermore, the signal integrity has to be maintained to ensure that receiver circuits in digital interfaces can sample the incoming data without errors. The following chapters are clustered like the information in most datasheets for ESD protection devices by Nexperia.

2.1 Limiting Values

V_{RWM} is the standoff voltage of a protection device. It indicates the maximum operating voltage range for which leakage current is below a specified value I_{RM}. V_{RWM} has to be equal to or higher than the maximum voltage expected on a signal line.

I_{PPM} is the maximum surge current that a device can withstand if an IEC 61000-4-5 [5] pulse with an 8/20 µs timing is applied. This value gives an indication of the robustness of ESD devices if they are exposed to higher pulse energy, see Chapter 3.4.

For the junction temperature T_j, a maximum value is given which usually is 150°C. Beside this information, an ambient temperature range T_{amb} and storage temperature T_{stg} can be found with minimum and maximum limits.

2.2 ESD maximum ratings

V_{ESD} gives the maximum voltages that an ESD protection device can withstand, in compliance with IEC 61000-4-2 [6], see Chapter 3.1. The limits in kV are given for positive and negative ESD test pulses. The datasheets give limits for contact discharge testing as well as for air discharge testing. For low capacitance protection devices, the air discharge rating is not significantly higher than the contact discharge rating. Designers should rely on the contact discharge rating because this is much better in reproducibility. The ESD rating does not indicate if a protection device will provide good protection for an interface. It has no correlation to the ESD system robustness that can be achieved. In the best case, the overall system robustness is limited by the ESD robustness of the ESD protection device.

However, this is not the case in most applications if sensitive interface pins have to be protected. If the system chip is damaged with an 8 kV ESD pulse in a system test, it does not help that an ESD diode with a +/– 30 kV rating was applied. A low clamping protection diode rated for e.g. 15 kV can be the far better choice.

2.3 Characteristics

The diode capacitance C_d is an important parameter related to the maximum frequency of a signal line. The value is given for a test frequency of usually 1 MHz and no bias; sometimes, additional values with bias voltage are provided. A bias voltage leads to lower C_d values because the capacitance of internal pn-junction, decrease with reverse voltage.

f_{-3dB} is the −3 dB frequency of the insertion loss tested at a sine-wave generator with 50 Ω output resistance. Figure 2 shows an example for an insertion loss curve with a −3 dB cut-off frequency of about 17 GHz. For data interfaces, at least the fundamental wave should pass without big losses. To achieve steeper transitions, it is essential to have a significant spectral component for the 3rd harmonic as well.

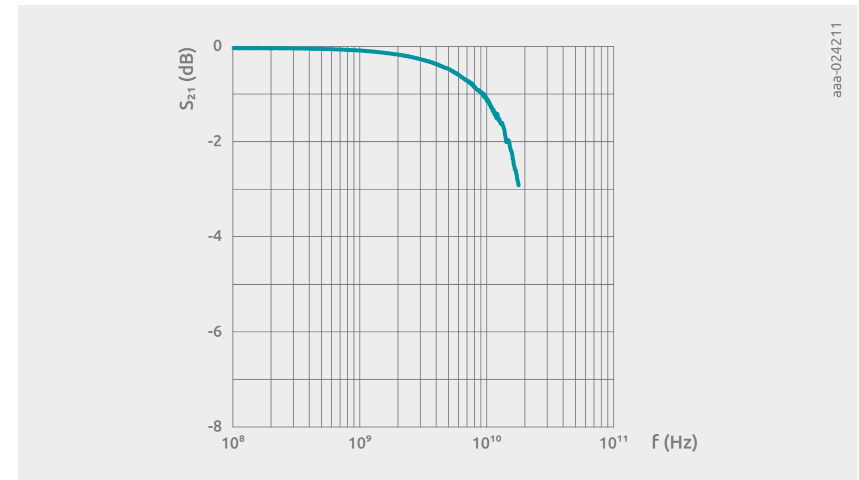


Figure 2 | S_{21} insertion loss curve of PESD3V3Z1BSF

V_{BR} is the breakdown voltage of a protection device. It is tested with a current-driven set-up in which 1 mA test current is driven through the device under test (DUT). The voltage across the DUT is V_{BR}.

For a topology similar to an ordinary Zener diode, this parameter is of practical interest as it indicates the voltage at which leakage current will reach 1 mA. However, for ESD protection that has a snap-back topology but not static behavior, V_{BR} can be misleading. ESD protection devices with an open-base topology have very low leakage currents below 1 mA before the trigger voltage is reached. The current-driven test approach for V_{BR} forces such devices into snap-back. In this case V_{BR} is lower than the trigger voltage and V_{RWM} can be higher than V_{BR} in principle.

I_{RM} is the leakage current at V_{RWM}. It is typically extremely low, at 1 nA and a maximum rating of 50 nA.

V_{CL} are clamping voltages for IEC 61000-4-5 pulses for different peak currents I_{pp}. Usually V_{CL} is given for the limiting I_{pp} value and additional lower values.

R_{dyn} is the so called dynamic resistance. For modern devices this parameter is defined by the steepness of the TLP curve for TLP pulses with 100 ns pulse width at I_{PP} ~ 16 A. The lower the dynamic resistance of a protection device, the better is the clamping performance. This is because the clamping voltage increases less for rising surge currents. In many datasheets, dynamic resistances are given based on IEC 61000-4-5 (8/30 µs pulses) test results. The value is derived from an I_{PP} versus clamping voltage curve for such a test. When comparing dynamic resistances, attention has to be paid to the test method, because the values are not identical for the two approaches due to the significantly higher energy of IEC 61000-4-5 pulses towards TLP testing.

S-parameters

A scattering, or S-parameter, matrix is a mathematical approach that quantifies how radio frequency (RF) energy propagates through a multi-port network. The S-parameter matrix allows the properties of a complicated network to be described as a simple black box with n ports. The matrix for a network with n ports contains n^2 coefficients, each of them representing a possible path.

S-parameters are complex numbers containing real and imaginary parts, or a magnitude and phase part. The network changes both the magnitude and phase of the incident signal. S-parameters are defined for a given frequency and a defined system impedance Z_0, which is 50 Ω for datasheets and Nexperia laboratory testing. S-parameters are measured over a chosen frequency range and vary over frequency, as Figure 2 shows with the example of an S_{21} parameter curve.

S-parameters are usually depicted in a matrix format. The number of rows and columns is equal to the number of ports. For the S-parameter S_{mn} the n subscript stands for the port that is excited, as input port. The m subscript stands for the output port. This means S_{11} describes the reflection on port one: It is the relativ signal amplitude that is reflected. Parameters in the S-matrix diagonal are the reflection coefficients, while those located off the diagonal are called transmission coefficients. They describe how the network reacts at a port if it is excited with an incident sinewave from another port. The parameter S_{21} is often referred to as insertion loss. The parameter S_{11} is often referred to as return loss.

S-parameters describe the response of an n-port network to a signal incident to any or all of the ports.

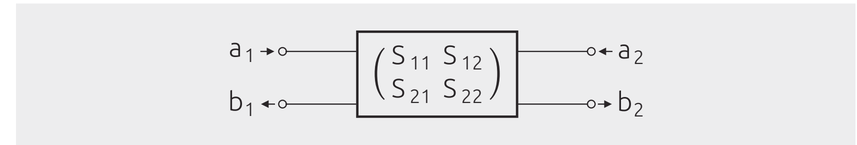


Figure 3 | 2-port network with 4 nodes and direction indication arrows

Figure 3 shows a 2-port network. The signal at a port, for example port 1, can be thought of as the superposition of two waves running in opposite directions. By convention, each port is shown as two nodes so as to give a name and value to these opposite direction waves. The variable a_m represents a wave incident to port m and the variable b_n represents a wave reflected from port n. From the matrix formula below the following equations are valid for the four S-parameters of the 2-port network:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

$$S_{11} = \frac{b_1}{a_1},\ S_{12} = \frac{b_1}{a_2},\ S_{21} = \frac{b_2}{a_1},\ S_{22} = \frac{b_2}{a_2}$$

For differential signals, mixed-mode S-parameters are used. The two signal lines are defined as ports. This way, a 4-port network is created. By simple mathematical operations the so called single ended representation can be transformed to mixed-mode. In this representation, differential and common-mode signals are the ports. This is very useful when accessing unwanted differential to common mode conversion.

Chapter 3

ESD testing standards and TLP testing

3.1 ESD testing standard IEC 61000-4-2

IEC 61000-4-2 defines test methods and configuration environment for ESD robustness testing [6]. It is commonly used to certify electronic equipment. Devices must be protected against ESD using components that can clamp and resist the high voltages, as defined by the respective IEC standards. The robustness of these devices has to be checked and guaranteed. The tests defined in the standard are system level ESD tests in the context of EMC compliance testing.

Most electrostatic discharges occur unnoticed by users but can seriously damage gate oxides of MOSFETs used in the data path of most interfaces. In some cases, a small flash indicates that a sudden electrical discharge has occurred. The after-effects are high leakage currents and malfunction of input and output circuits.

Contact and rubbing of different materials causes seperations of charger by means of the socalled triboelectric effect. Furthermore, electrostatic induction leads to a redistribution of electrical charge in an object caused by the influence of nearby charges.

Please note that when ESD protection components are mounted in a product to protect some of its sensitive parts, the behavior of these components must be tested in their final application environment. ESD pulses are generated with an ESD gun that consists of an adjustable high voltage source with maximum of 30 kV. A 150 pF capacitor is charged through a resistor with 50 to 100 MΩ, using a charging switch. The capacitor is discharged through a 330 Ω resistor when the discharge switch is closed. Figure 4 shows a basic ESD pulse generator schematic.

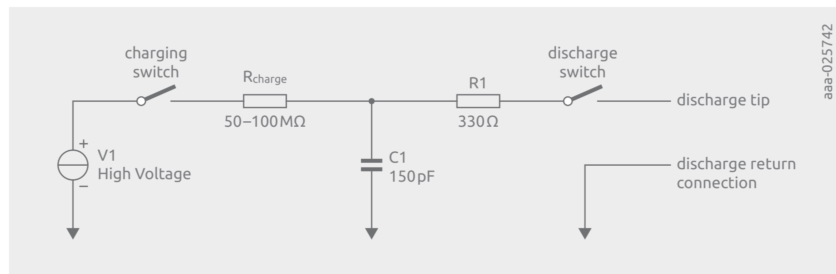


Figure 4 | ESD pulse generator according to IEC 61000-4-2

Figure 5 shows the shape of the IEC 61000-4-2 discharge current waveform of the described generator. The curve behaves in the following way:

1. The pulse rises within 0.7 to 1 ns.
2. The first spike reaches its peak current with the peak value I_{PP}.
3. The pulse then declines within about 80 ns including a shoulder-shape curve.

Most of the surge pulse energy is carried by the shoulder. The first spike stresses the target with high voltage and high current, but with less energy because duration is short. Two methods are used for ESD testing: The contact measurement method and the air discharge measurement method.

The contact measurement method is the recommended IEC 61000-4-2 method for ESD protection components and is set-up as described below:

- The ground pin of the component is connected. The ESD gun is connected to ground via the discharge return connection as well.
- The tip of the ESD gun is connected to the contact of the DUT.

In contrast to the system level testing described in IEC 61000-4-2, the test procedure of ESD protection devices does not employ resistors (2 × 470 kΩ) in the return path. The contact discharge connection allows good reproducibility of test results. Further details on the test procedure can be found in [7].

Table 1 lists current values for predefined IEC 61000-4-2 levels, i.e. ESD levels 1 to 4, for respective peak currents, 30 ns and 60 ns.

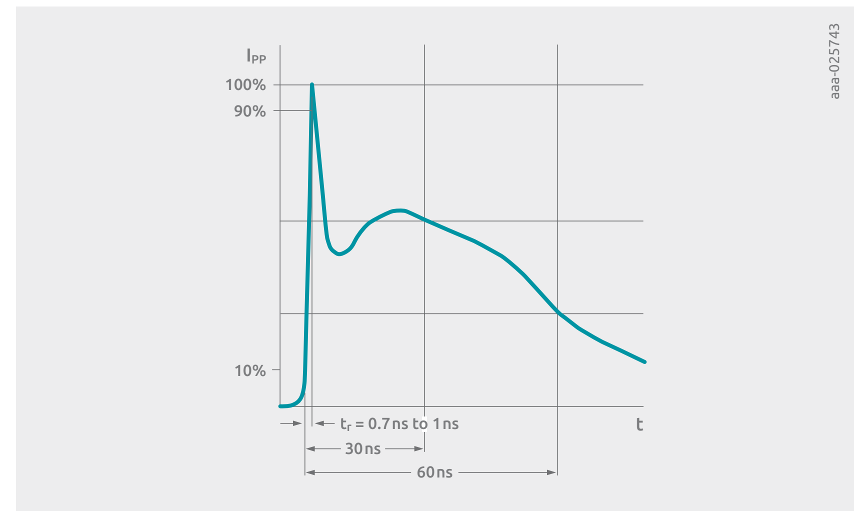


Figure 5 | IEC 61000-4-2 waveform

Table 1: ESD test waveform parameters

ESD level	voltage	first peak current, +/– 10%	Current (+/– 30%) at 30 ns	Current (+/– 30%) at 60 ns
1	2 kV	7.5	4	2
2	4 kV	15	8	4
3	6 kV	22.5	12	6
4	8 kV	30	16	8

Table 2 shows the definition of IEC 61000-4-2 ESD levels with the related minimum discharge voltages for contact discharge testing.

Table 2: ESD levels as defined in IEC 61000-4-2

ESD level	contact discharge	air discharge
1	2 kV	2 kV
2	4 kV	4 kV
3	6 kV	8 kV
4	8 kV	15 kV

For air discharge the tip of the ESD gun is narrowed slowly towards the target until a flash strikes over. The results depend very much on air humidity, speed of decreassing distance between target and gun, and shape of electrodes. Generally this test shows low reproducibility. Often, corona discharge can be noticed without a flash if one of the two electrodes has a sharp end. In such a case, the stress on the ESD device is very low and does not lead to usable results. For the gun side a tip with a round end is defined for air discharge, whereas the tip for contact discharge has a sharp end. The air discharge waveform has a less steep rising edge and the surge pulse peak values are lower. Therefore, **air discharge robustness is higher than, or equal to, contact discharge**.

Please note that technical documents must be regarded with skepticism if air discharge ratings are presented with much higher values than for contact discharge. Often, a factor of roughly 2 like the ESD level 4 definition in Table 2 is presented. Please note that the voltage levels do not imply each other, but are just categorizations for practical usage. Moreover, the levels defined in [6] refer to system level testing rather than device level. It is a proven fact that for low capacity ESD protection devices the air discharge robustness is a few kV higher or the same compared to contact discharge robustness. For this reason air discharge testing is discouraged not recommended, because it is much more difficult to do it correctly and, if done correctly, it provides exactly the same results as contact testing [8].

Human Metal Model (HMM) test uses the same waveform as defined for ESD guns in standard and supports 50 Ω terminated testing of ESD protection products and interfaces. The defined termination guaranties good reproducibility of test results as known from TLP tests.

3.2 Reproducibility aspects for IEC 61000-4-2 testing

Figure 6 shows that the ESD gun waveform is not fully reproducible: Here, a NoiseKen gun[1] is shooting in repeat mode at a target while a high frequency current probe[2] is measuring the current waveform. The second peak, which is located on the shoulder behind the first peak, is stable and is well within the IEC 61000-4-2 specification. However, the voltage of the first peak shows a big variation from +25% to −35%. If target systems are sensitive to the first peak of an ESD event, test results can show a big spread which can lead to wrong decisions being taken in the selection process of protection devices. Guns of other manufacturers show simular behaviour.

1 ESS2000AX
2 F-65 current probe 1 MHz–1 GHz from Fischer Custom Communications

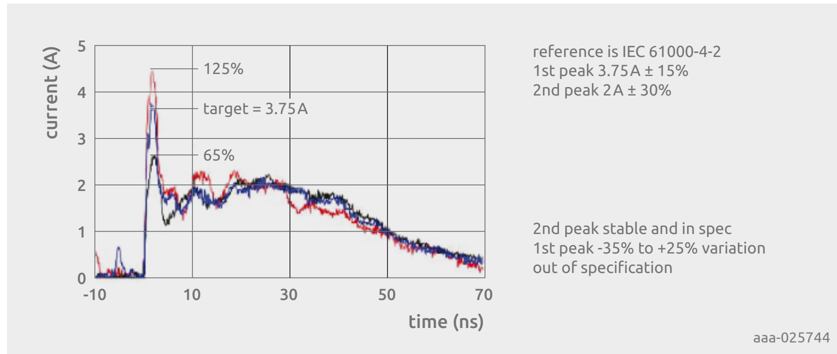


Figure 6 | IEC 61000-4-2 waveforms with NoiseKen ESS2000AX gun

Please note that the grounding condition has a big impact on the voltage level of the first peak as well. If there is no proper ground close to the DUT, a small residual capacitance to ground occurs. If this is the case, the first peak loses its height and can mostly disappear. Figure 7 shows the current waveforms of two ESD gun[3] types with and without proper grounding. In set ups without proper grounding test results are unreliable.

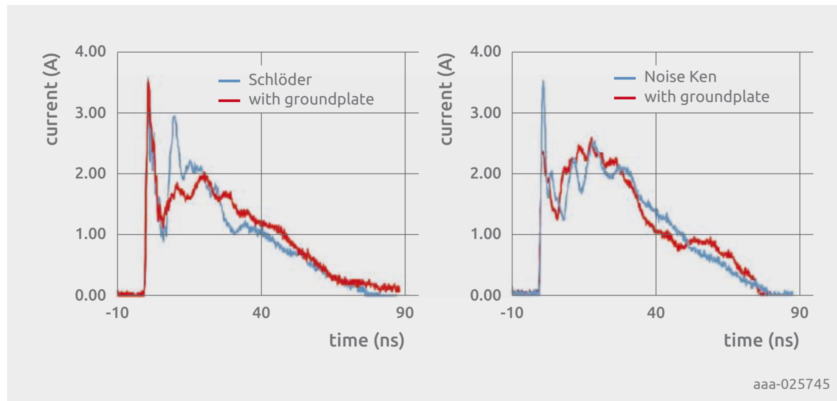


Figure 7 | Waveform comparison for ESD gun with and without proper grounding

Another risk in ESD gun testing arises when the gun is not safely connected to the DUT for contact discharge. Figure 8 shows the circuit of an ESD gun with a parasitic tip capacitance C_t of roughly 40 pF, which is significant compared to the nominal 150 pF of the ESD gun.

3 A SESD 30.000 from Schlöder and a ESS2000AX from NoiseKen

When a triggered gun misses the target or when the charge moves across the switch S2, the C_t charge can discharge into the DUT with almost no series impedance. This is why the first peak of this socalled stray pulse can exceed the regular pulse by a factor of 2, as illustrated by the red curve in the diagram.

In conclusion, if a system is tested that shows an ESD sensitivity on the first peak, unsafe ESD gun connection can lead to damage at a comparatively low testing voltage, wrong test results, and ESD device selection. A propper test setup is essential to ensure reproducibility of ESD testing. More details about system level ESD testing of high-speed interface boards can be found in [7] and [8].

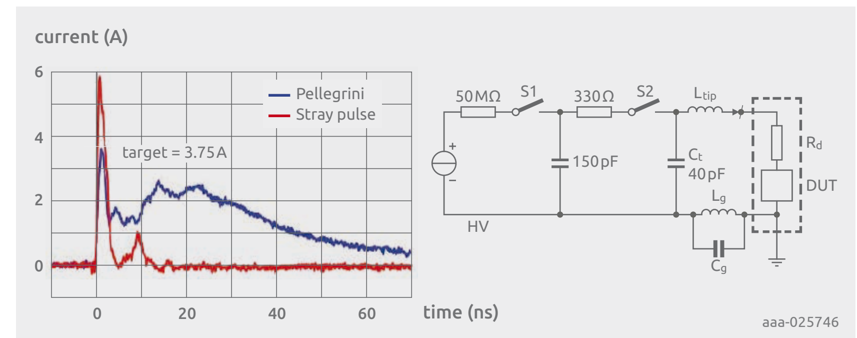


Figure 8 | Stray pulses after the target was missed

3.3 ESD testing standard ISO10605

Besides the IEC61000-4-2 ESD testing standard, ISO10605 is the common ESD testing standard in automotive. It is partially based on IEC61000-4-2 and describes various procedures to capture ESD during assembly of the car, during maintenance, and from the passenger. For the rating of ESD protection and transient voltage suppressor (TVS) devices, the waveform is of interest.

The underlying discharge network is similar to the one of IEC61000-4-2, as shown in Figure 4, with capacitance C1 of 150 or 330 pF and resistances R1 of 330 and 2000 Ω. For the rating of protection device, the more severe pulse with R1 = 330 Ohm is common and both capacitor values are tested. The variant with 330 pF is more severe.

In contrast to IEC61000-4-2, the ISO10605 demand to ground the ESD generator at the car battery instead of the table. As for device tests, only contact discharge is evaluated and there is no powered case, the test setup and procedure is equal to IEC61000-4-2 besides the used ESD generator.

3.4 Surge testing standard IEC 61000-4-5

Testing according to IEC 61000-4-5 [5] uses much wider test pulses than in the ESD testing according to IEC 61000-4-2 [6] discussed in the previous chapter. The energy of surge pulses, as defined in [5], is much higher. Consequently, an ESD protection part has to dissipate more heat. The IEC 61000-4-5 standard approach simulates surge events, for instance in scenarios like power supply voltage overshoots created by load changes or overshoots caused by the plug-in procedure of chargers.

Table 3 lists key waveform data of IEC 61000-4-5 surge pulses. For the short-circuit condition of the surge generator, see Figure 9, 8 μs rise time and 20 μs fall time to 50% voltage level are defined and is well known as the 8/20 μs surge test.

Table 4 lists the relation between selected values of the peak voltage for the open circuit condition, see Figure 10, and the peak current for the short circuit case. Output impedance of a surge generator is considered to be 2 Ω.

Table 3: Surge pulse waveform parameters

operating mode	Front time in μs	time down to 50% value in μs
open-circuit voltage	1.2 +/− 30%	50 +/− 20%
short-circuit current	8 +/− 20%	20 +/− 20%

Table 4: Open-circuit peak voltage and related peak current for the short-circuit

open circuit peak voltage +/− 10%	short-circuit peak current +/− 10%
0.5 kV	0.25 kA
1.0 kV	0.50 kA
2.0 kV	1.00 kA
4.0 kV	2.00 kA

Figure 9 shows the waveform for the short circuit condition, whereas Figure 10 depicts the surge pulse waveform for the open circuit scenario.

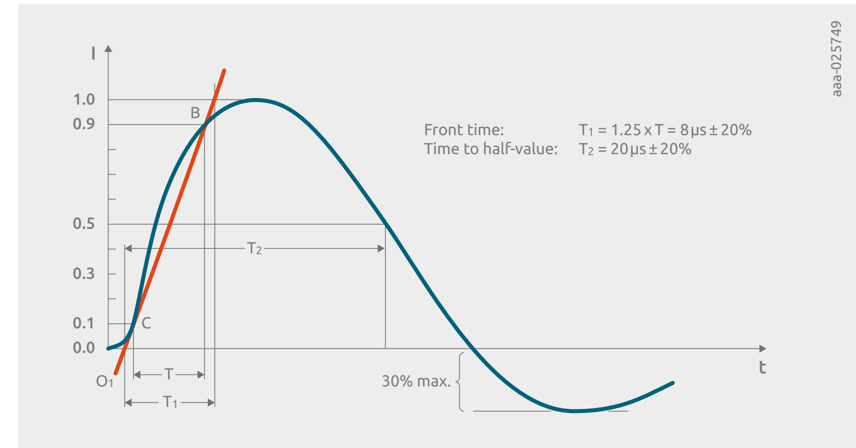


Figure 9 | IEC 61000-4-5 waveform for short circuit condition

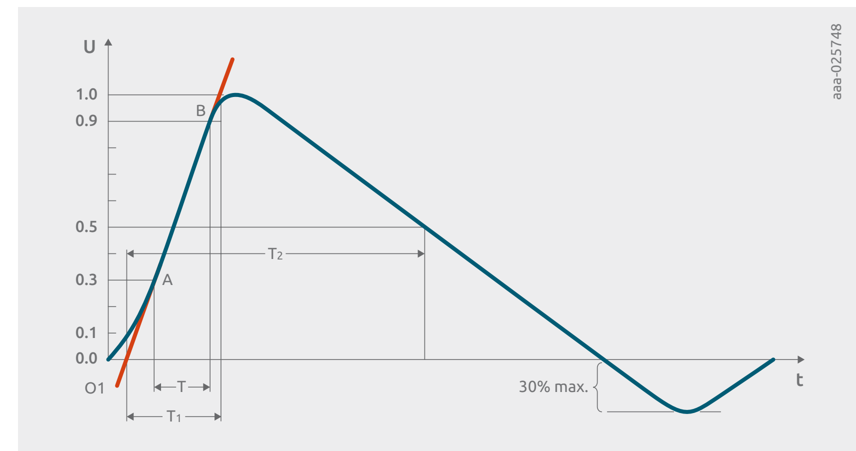


Figure 10 | IEC 61000-4-5 waveform for open circuit condition

IEC 61000-4-5 test results deliver important data sheet parameters for ESD and surge protection devices:

- Maximum surge current — I_{PPM}
- Peak power — P_{PP}
- Clamping voltage — V_{CL}
- Dynamic resistance — R_{dyn} — derived from the steepness of V_{CL} versus I_{PP} curves

3.5 Automotive transients ISO7637-2 and ISO16750-2

The standards ISO7637-2 [9] specify test procedures for compliance immunity to transients on supply lines for automotive ECUs. As the pulses are only considered on the supply line and not on the data line, external ESD protection devices generally do not have to comply. However, in some circumstances of harsh environment, car OEMs require protections for in-vehicle networking busses to also fulfil the requirements partially. Large TVS diodes that are used to protect the supply line in automotive are often required to comply, even though the norm specify system level requirements. The ISO7637-2 is defining several test pulses. The pulses 5a and 5b have been shifted to ISO16750-2 under the name of load dump.

The ISO16750-2 [10] describes the effects of electrical loads in a vehicle and how to test the DUT for compatibility. This includes various operational conditions that are not of relevance for TVS or ESD protection devices. Here, the effect of resistive behavior from the load and the resulting parasitic of the wiring harness and jumpstart condition are covered.

3.5.1 ISO7637-2 Pulse 1: Disconnecting an inductive load

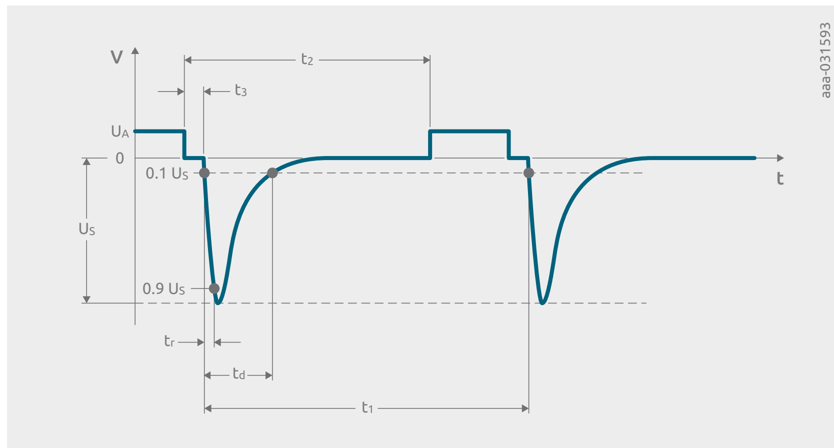


Figure 11 | Waveform of Pulse 1, disconnecting an inductive load

Pulse 1, shown in Figure 11, is representing a negative transient seen by a load parallel to an inductive load in the event of a disconnection of the power supply. The defined parameter range is very large and often corner configurations are tested to assess worst case configurations. Table 5 provides the parameter ranges and typical configurations these parameters are different for 12 V and 24 V boardnet.

Table 5: Parameter ranges for Pulse 1 shown in Figure 11

Board net	Ua (V)	Us (V)	Ri (Ω)	td (ms)	tr (μs)	t1 (s)	t2 (ms)	t3 (us)
12 V	13.5±0.5	-75 to -150	10	2	0.5 to 1	> 0.5	200	< 100
24 V	27 ± 0.5	-300 to -600	50	1	1.5 to 3	> 0.5	200	< 100

3.5.2 ISO7637-2 Pulse 2a: Interruption of power supply

Pulse 2a, shown in Figure 12, represents the parasitic inductance of the wiring harness. These inductance forces a positive voltage peak into the supply line of the DUT when it draws current and the voltage supply is interrupted. The parameter ranges are listed in Table 6.

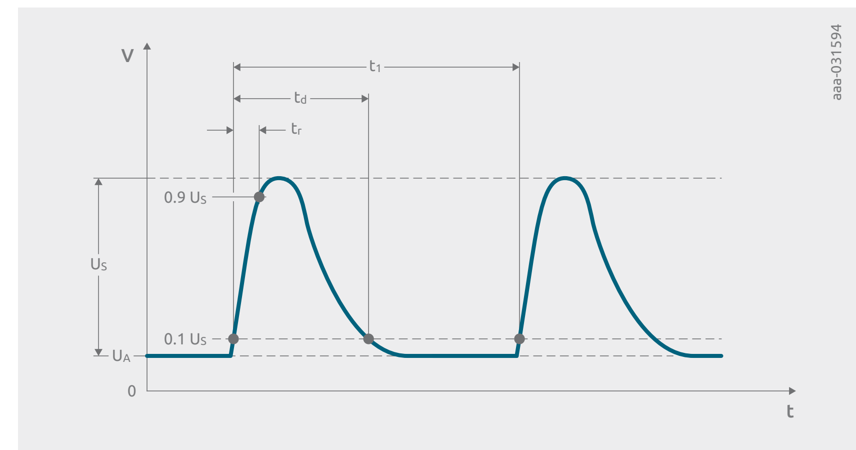


Figure 12 | Waveform of Pulse 2a, interrupted power supply

Table 6: Parameter ranges for Pulse 2a shown in Figure 12

Board net	Ua (V)	Us (V)	Ri (Ω)	td (ms)	tr (μs)	t1 (s)
12 V	13.5 ± 0.5	37 to 112	2	0.05	0.5 to 1	0.2 to 5
24 V	27 ± 0.5	37 to 112	2	0.05	0.5 to 1	0.2 to 5

3.5.3 ISO7637-2 Pulse 2b: DC motors as unintended generators

Pulse 2b, shown in Figure 13, represents the effect of an energy sink acting as a source. This can occur e.g. when mass is moved by an electric motor. A good example is the blower fan and or the windshield wipers. In both cases mass is moved. When the ignition is turned off the mass remains moving for some time and in this moment the electric motor acts as a generator. The parameter ranges are listed in Table 7.

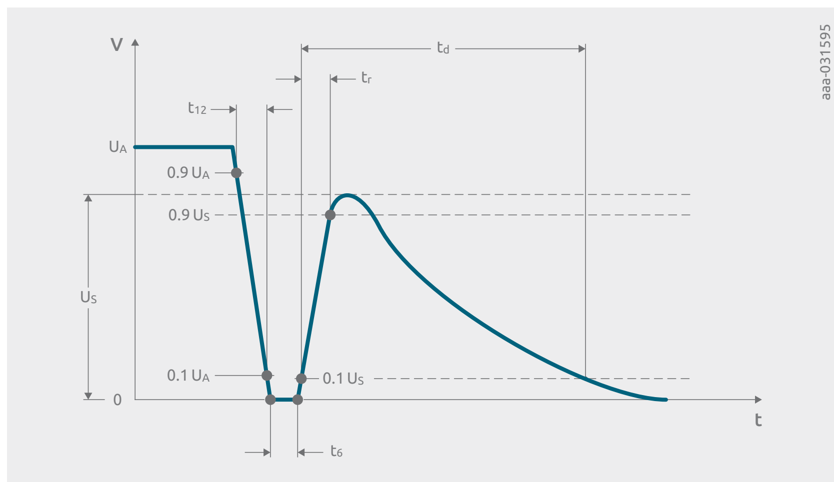


Figure 13 | Waveform of Pulse 2b, DC motors as unintended generators

Table 7: Parameter ranges for Pulse 2b shown in Figure 13

Board net	Ua (V)	Us (V)	Ri (Ω)	td (ms)	tr (ms)	t12 (ms)	t6 (ms)
12 V	13.5 ± 0.5	10	0 to 0.05	0.2 to 2	1 ± 0.5	1 ± 0.5	1 ± 0.5
24 V	27 ± 0.5	20	0 to 0.05	0.2 to 2	1 ± 0.5	1 ± 0.5	1 ± 0.5

3.5.4 ISO7637-2 Pulse 3a and 3b: Fast transients

Pulse 3a and 3b, shown in Figure 14 and 15, respectively, and are rarely used. They represent fast transients – Pulse 3a negative and Pulse 3b positive – in the power supply of the DUT. These transients can occur every time when electrical load is switched on or off. The connected wiring harness and its parasitic inductance and capacitance or the bouncing of a relay or switch a cause very fast voltage peaks on the supply line. Compared to Pulses 2a and 2b this pulse is much faster with a higher amplitude Us but lower energy. Occationally, robustness against this pulses is also requested for external ESD protection devices for CAN or LIN. The parameters are listed in Table 8.

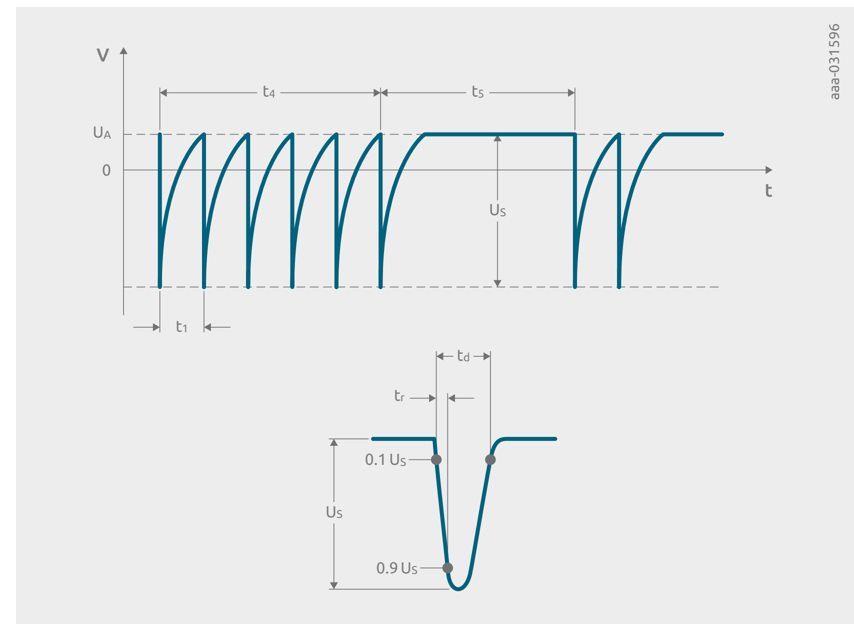


Figure 14 | Waveform of Pulse 3a, negative fast transient

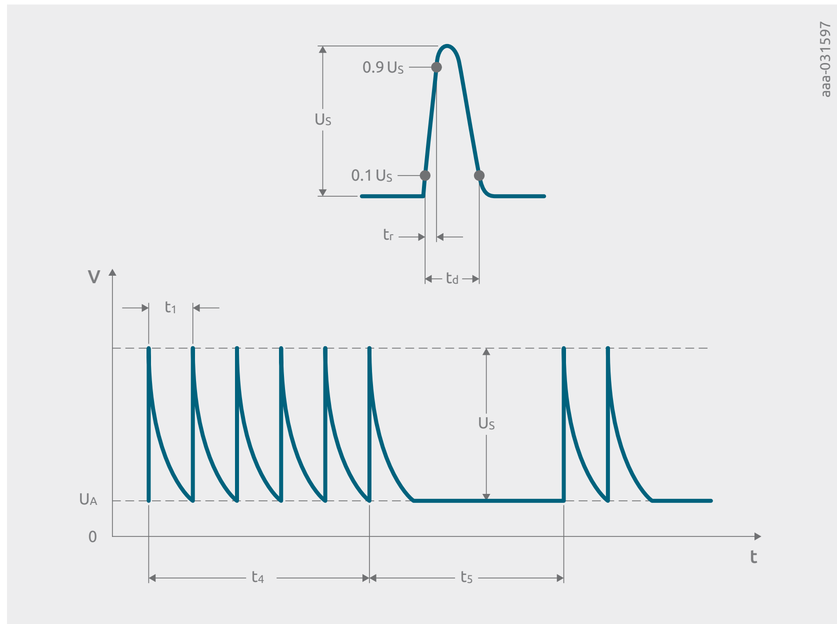


Figure 15 | Waveform of Pulse 3b, positive fast transient

Table 8: Parameter ranges for Pulses 3a and 3b shown in Figures 14 and 15

Board net	Pulse	Ua (V)	Us (V)	Ri (Ω)	td (ns)	tr (ns)	t1 (µs)	t4 (ms)	t5 (ms)
12 V	3a	13.5±0.5	-112 to -220	50	150±45	5±1.5	100	10	90
12 V	3b	13.5±0.5	75 to 150	50	150±45	5±1.5	100	10	90
24 V	3a	27±0.5	-150 to -300	50	150±45	5±1.5	100	10	90
24 V	3b	27±0.5	150 to 300	50	150±45	5±1.5	100	10	90

3.5.5 ISO16750-2 §4.3 Overvoltage

When jumpstarting a car significantly higher voltages than the nominal supply voltage can be applied. As all ECUs are supplied from the same grid, all systems of the car need to be able to withstand these over voltages. In a 12 V system the DUT has to withstand 24 V for 60 ± 6 seconds and in a 24 V system 36 V for 60 ± 6 seconds. This test is also performed 20°C below maximum operating temperature.

3.5.6 ISO16750-2 §4.6.4 Load Dump

This test simulates the effect of an empty batterie which is disconnected while charging. An empty battery is charged by the alternator with a comparatively high current. If the battery is disconnected from the supply line during charging, the alternator will produce a voltage peak in the supply line supply. Two slightly different pulses can occur. These test pulses have previously been published as pulse 5a and 5b in ISO7637-2 and have been shifted to ISO16750-2 later. The first pulse, see Figure 16, simulates the voltage peak without suppression.

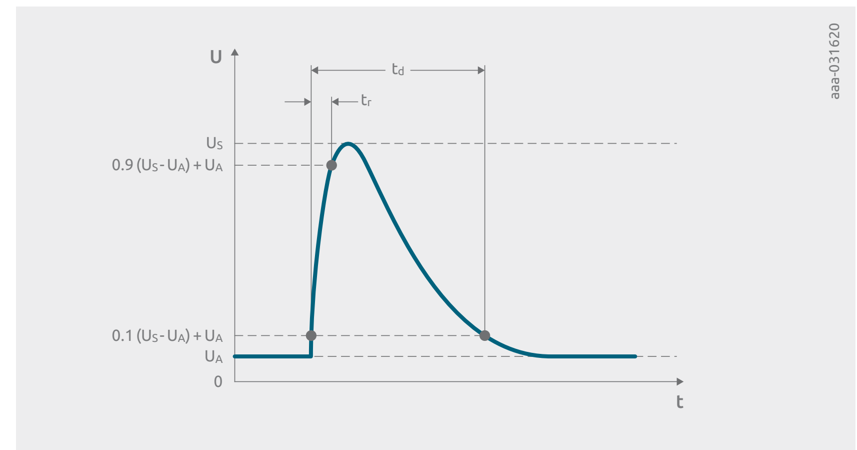


Figure 16 | Waveform of load dump without suppression according to ISO16750-2

Figure 17 is showing the pulse with a load dump suppression. In this case, the pulse is limited to the value Us* by a centralized load dump suppression. This can be implemented by using a large TVS diode. The parameter range are listed in Table 9.

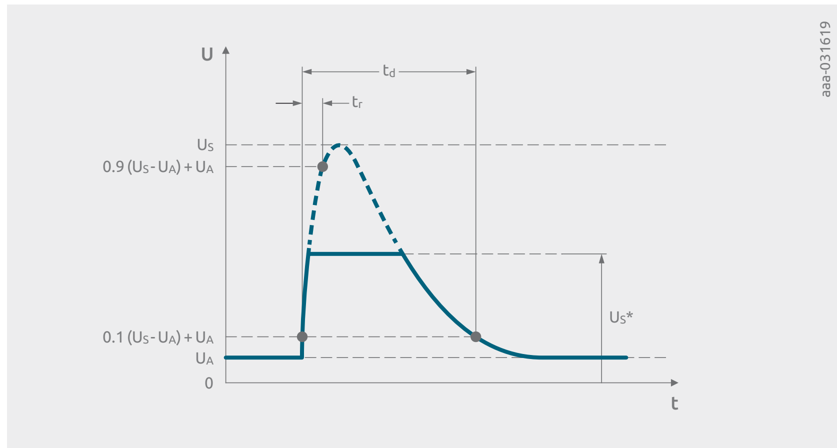


Figure 17 | Waveform of load dump with suppression according to ISO16750-2

Table 9: Parameter range for load dump

Board net	Us (V)	Us* (V)	Ria (Ω)	td (ms)	T3 (ms)
12 V	79 to 101	35	0.5 to 4	40 to 400	5 to 10
24 V	151 to 202	Not specified	1 to 8	100 to 350	5 to 10

3.6 TLP – Transmission-line Pulse testing

TLP is a comparatively new measurement technique used to characterize complete interfaces or ESD protection components [11, 12].

TLP is a short-duration rectangular pulse in a controlled impedance environment of 50 Ω, which improves test accuracy and measurement reproducibility. TLP characterizes performance attributes of devices under stresses that have a short pulse width and fast rise time. Low duty cycles prevent heating.

The TLP test environment shown in Figure 18 can be described as follows: a generator charges a 50 Ω transmission line with a pre-adjusted voltage. The switch is closed and the energy is applied to the DUT. The current into the DUT measured by a current probe, while the voltage at the DUT is monitored using a high-speed oscilloscope. The pulse length, rise, and fall times can be changed at the generator. Typically, the standard pulse applied has a 100 ns duration and rise and fall times of 10 ns each. The minimum programmable transition times are 300 ps.

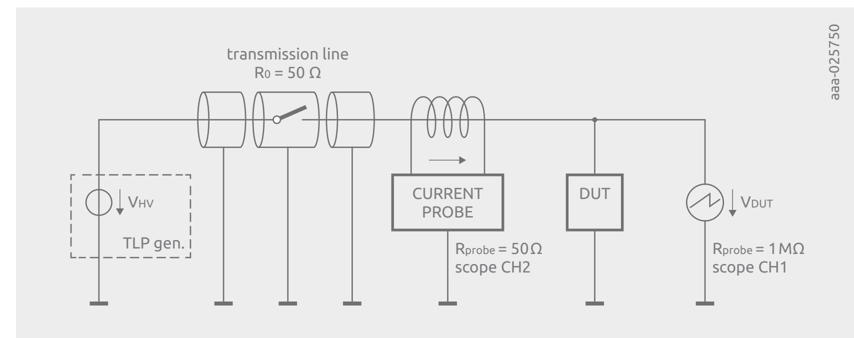


Figure 18 | TLP test set-up

The TLP test is performed starting gradually from low pulse voltages to higher voltages, with a pre-defined step width. As shown in the TLP measurement voltage and current traces depicted in Figure 19, the voltage and current samples are averaged for a window of 20 ns. Located in a temporal window from 70 ns to 90 ns within the 100 ns test pulse, the window-based method eliminates noise. Also, the window's location ensures that the system is settled so that run-in effects like overshoots are eliminated. Each measurement result becomes a point on the TLP graph that shows a TLP I-V characteristic, i.e. the TLP-curve.

The steepness of the TLP curve ΔV/ΔI is the R_{dyn}, which is an important parameter for selecting ESD and surge protection devices.

TLP testing can be done with ESD protection devices, and with interface pins of complete systems with and without ESD protection. From the derived TLP curves conclusions can be drawn as to which protection device is suitable to protect a product safely and reliably.

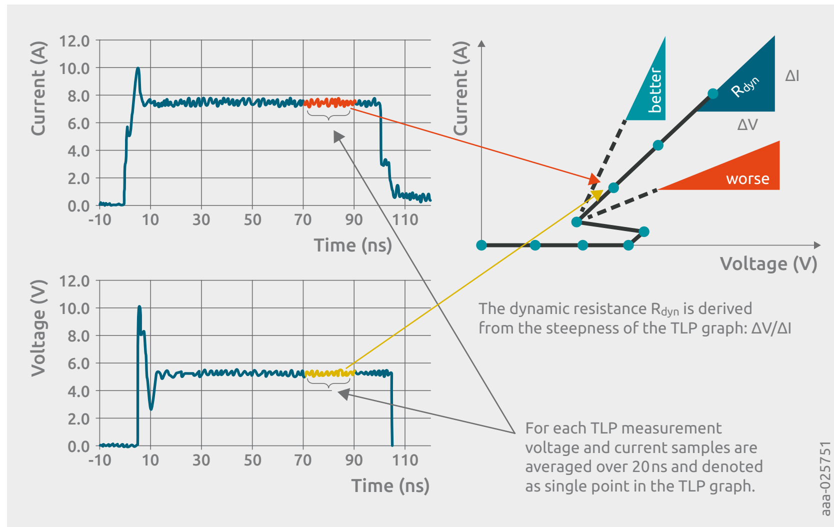


Figure 19 | TLP curve derived from TLP test events

3.7 VF-TLP – Very fast TLP testing

A very similar testing method to TLP is very-fast TLP (VF-TLP) [13]. The major differences being the 1 to 10 ns duration of the test pulses and the short rise and fall times of 100 to 600 ps.

Figure 20 shows the VF-TLP measurement set-up. Due to short pulses, the current is not measured with a current probe. Instead, it is derived from measuring incident and reflected voltages separately with an oscilloscope. This is done in a similar way to time domain reflection (TDR) measurement. The current in the DUT is calculated using:

$$I_{DUT} = I_{incident} + I_{reflected} = \frac{V_{incident} - V_{reflected}}{50\ \Omega}$$

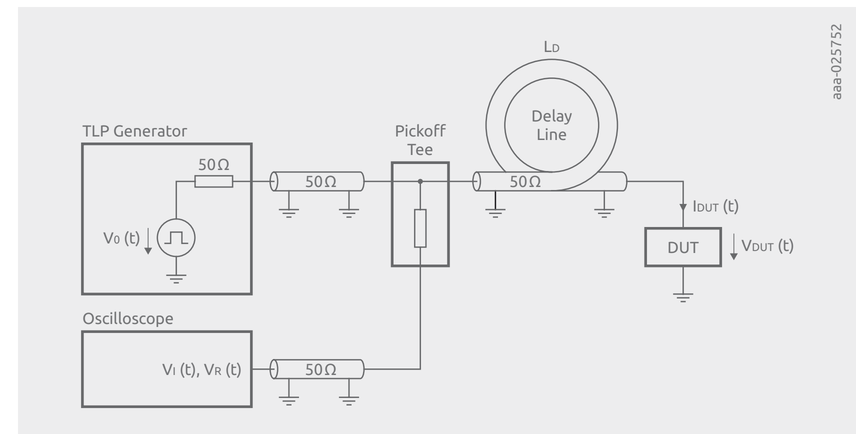


Figure 20 | Test set-up for VF-TLP measurement

In conclusion, VF-TLP tests provide a good indication for determining the switching speed of ESD protection devices. The small pulse length is useful because the impact of the first overshoot of an ESD event on a target system can be investigated.

In contrast to that, the 100 ns standard TLP pulses are roughly equivalent to the energy of a complete ESD pulse, in which the larger proportion of energy is carried in the wider second shoulder of the pulse.

Chapter 4

Principles of ESD protection

Several different approaches can be used to protect electronic devices against ESD and surge events.

- **Narrow gap or spark gap approach**
  An easy and inexpensive approach is to add a narrow gap from ground to signal line. Whenever a bigger ESD event occurs, an air discharge limits a high voltage pulse.
  Spark gap components operate on the same physical principal. Thus, adding a spark gap to a signal line is a straightforward approach. The disadvantage of this kind of ESD protection is comparatively poor performance in terms of the achieved clamping voltage that has a slow turn-on time and a very high trigger voltage. The average dielectric air strength is about 3.3 kV/mm. This is why spark gabs are rarely used in automotive applications and are not suitable to protect higher speed interfaces.
- **Use of varistors**
  Varistors are often used for ESD protection. These parts are made with ceramic ZiO grain material in a mixture with other metal oxides. Varistors have a symmetrical non-linear I-V curve which shows a high resistance for lower voltages. When the varistor reaches breakdown voltage, it starts conducting. Varistors deteriorate after exposure to surge events. Older generation varistors show a very high first spike in IEC 61000-4-2 testing, however newer generation varistors are much improved. Unfortunately, the clamping voltage for the second shoulder remains significantly higher compared to silicon-based solutions. Therefore, and because of degradation concerns varistors are not the first choice for protecting automotive interfaces.
- **Silicon-based ESD protection**
  Silicon-based ESD protection are the preferred choice as they show no degradation after surge events, as long as the specified limits are obeyed. Several topologies are available that provide ESD protection ranging from a simple topology to more sophisticated topologies, as presented in several scenarios on the subsequent pages.

Silicon-based ESD protection is recommended with best and lowest clamping voltage performance, as explained on the subsequent pages of this section.

4.1 Unidirectional ESD protection with a Zener diode

A very plain topology is a Zener diode placed between ground and signal line, as depicted in Figure 21. Surge pulses are clamped to a voltage V_{CL} that is based on the following V_{CL} equation:

$$V_{CL} = V_{BR} + I_{PP} \cdot R_{dyn}$$

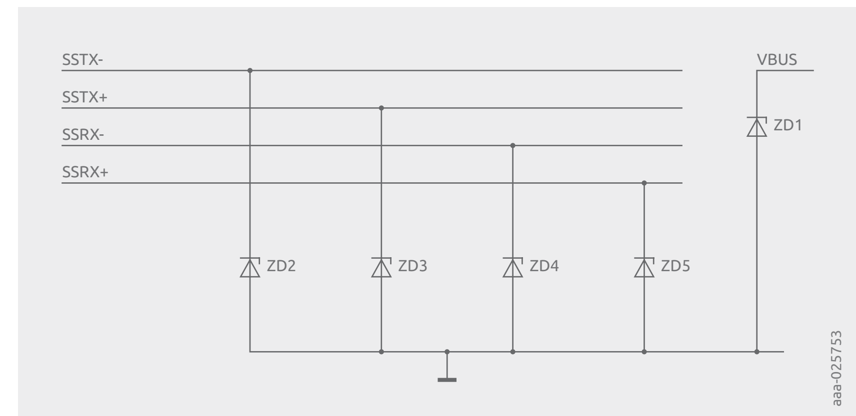


Figure 21 | ESD protection based on Zener diodes

Figure 22 shows a typical Zener diode I-V curve. The left side of the curve shows the Zener diode in the reverse bias region. The current is very small, as long as the test or operating voltage remains below V_{RWM}. V_{RWM} is referred to as stand-off working voltage. Below this voltage, reverse leakage current is smaller than the specified I_{RM}. When the voltage increases, current increases suddenly, at which the avalanche region begins; marked by the breakdown voltage V_{BR}. The breakdown voltage is measured in a current-driven test set-up that pushes 1 mA through the diode.

The right side of the curve shows the Zener diode in the forward bias region. The current is picking up if the voltage exceeds V_F. Negative surge pulses are clamped to relatively low voltages ($V_F \approx -0.7$ V). The described topology forms a unidirectional protection.

A Zener diode creates a unidirectional protection for an interface, clamping at considerably low voltages for negative surge events above V_F, as well as clamping voltage — according to the V_{CL} equation — for positive surge events.

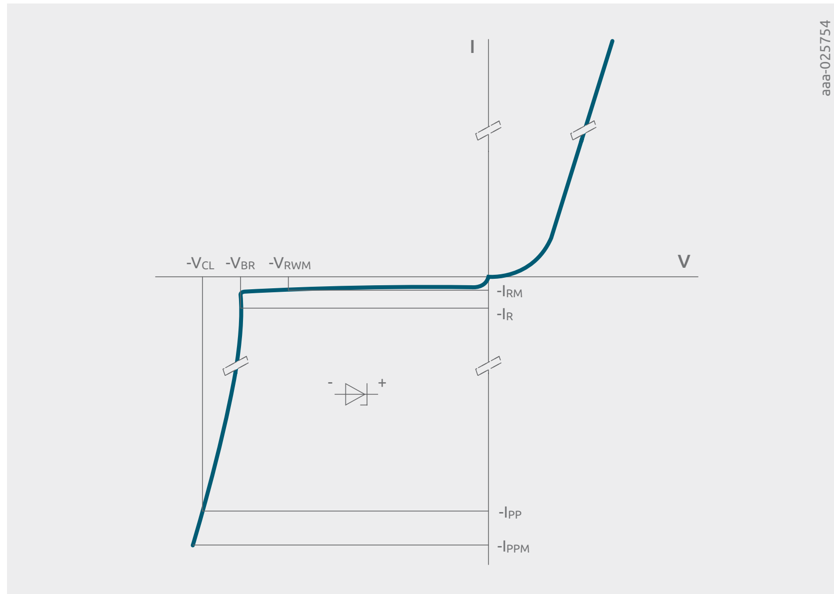


Figure 22 | I-V curve of a Zener-diode or avalanche type ESD protection diode

4.2 Bidirectional ESD protection with Zener diodes

If two Zener diodes with opposite directions are connected in a series, as shown in Figure 23, a bidirectional ESD device is created. If the two diodes are identical, the I-V curve is symmetrical, as depicted in Figure 24.

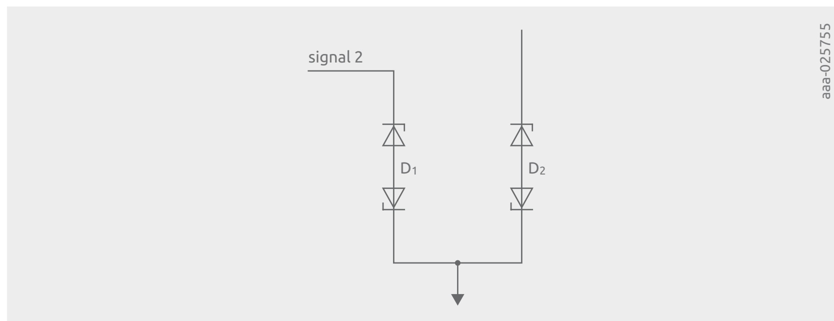


Figure 23 | ESD protection with a bidirectional ESD protection diode

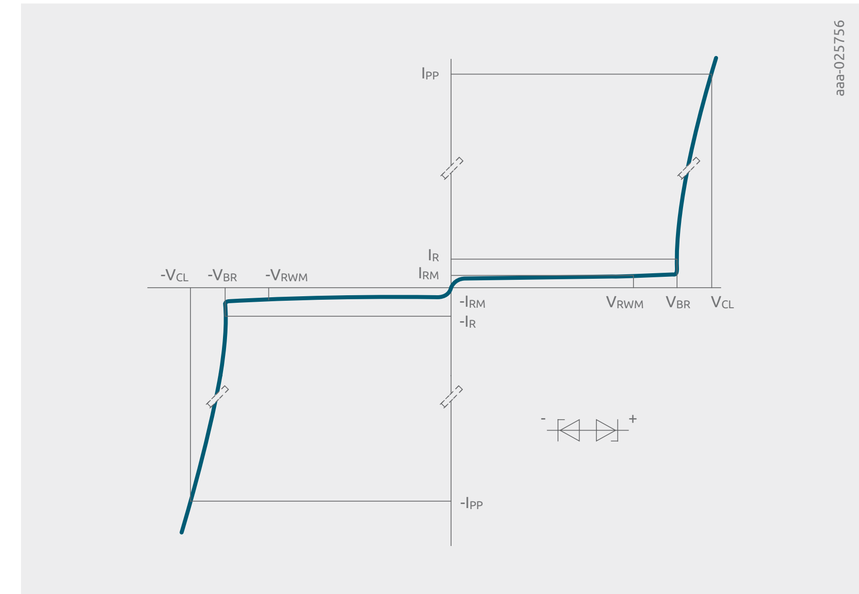


Figure 24 | I-V curve of a bidirectional ESD diode with a simple avalanche behavior

The calculation of the clamping voltage is the same as the equation for the reverse direction of unidirectional ESD diodes:

$$V_{CL} = V_{BR} + I_{PP} \cdot R_{dyn}, \text{ with } V_{BR} = V_{BR1} + V_F$$

The V_F value is adding a portion to V_{BR} and the reverse breakdown V_{BR1} of the other diode. Bidirectional ESD protection has to be applied to interfaces that operate with positive and negative voltage ranges. For example, analog audio signals. Most digital interfaces that only operate with positive voltages can be protected with a unidirectional solution. Anyhow, many designers make use of bidirectional ESD protection. The SoC are exposed to much higher negative clamping voltages for negative ESD strikes. This should be avoided if possible because it can badly affect the system level robustness. Especially for automotive in-vehicle networking interfaces, bi-directional protection devices are mandatory to comply with large voltage range allowed on the data line and to meet EMC requirements. The negative clamping behavior is no issue, as the SoCs are designed to withstand or additional circuitry, like common-mode chokes (CMCs) or ferrites are damping the amplitude additionaly.

When designing low capacitance ESD protection components it can be helpful to choose this structure with two ESD diodes in series because the parasitic capacitance is lower compared to a unidirectional device, as the below commonly known equation shows:

$$C_d = \frac{C_1 \cdot C_2}{C_1 + C_2}$$

Another reason for choosing bidirectional ESD diodes is that the mounting direction is not important.

4.3 Rail-to-rail topology with pn-diodes and Zener diode

Figure 25 shows an ESD protection environment with a rail-to-rail topology:

- From each signal line, one pn-diode is connected to the upper rail, while another pn-diode is connected from the signal node to the ground rail (GND)
- A Zener diode is connected between ground and upper rail
- Positive surge pulses push the energy through the upper diodes towards the upper rail
- Negative surge pulses push the energy through the lower diodes towards ground
- To improve the ESD performance, the upper rail can be connected to the supply voltage

The Zener diode functions as a clamping device and limits the voltage of positive surge events. If the upper rail is connected to a supply line or Vbus, current can flow into the supply as well where, typically, capacitors can damp incoming pulses. As a negative side effect, microcontroller circuits can show soft fails generated by the supply voltage overshoot created.

The rail-to-rail structure allows a very robust structure with a high capacitance of the Zener diode. The pn-diodes are comparatively small, with a small parasitic capacitance. C_d on the signal line is roughly twice the capacitance of the pn-diode, assuming that the top and ground rail works like a short circuit for RF components. This short is caused by the Zener diode's big capacitance and the comparatively big capacitors connected to the supply line. Therefore, rail to rail architectures are common to protect high-speed multimedia interfaces having a supply line, like USB. For IVN, where there is no supply line, the topology is used to reduce the capacitance only.

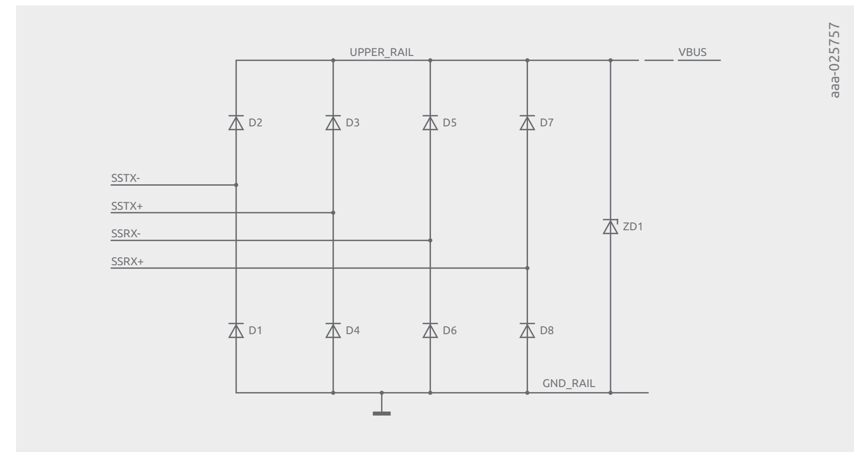


Figure 25 | ESD protection with rail-to-rail topology

4.4 Bidirectional ESD with open-base technology

In automotive applications, very often bidirectional behavior of external ESD protection devices is desired. The classic way of achieving this behavior is with cascaded Zener diodes. This approach is straight forward but also baring some drawbacks: The clamping behavior in terms of break down voltage and dynamic resistance is always worth than the one of the unidirectional Zener. Furthermore, the physical implementation can hit boundaries and increase cost significantly, as usually an additional piece of silicon and an additional bond wire is required.

Open-base technology incorporates the bidirectionality in one piece of silicon. The underlying principle is a bipolar transistor-like structure, with an unconnected base. Upon an overvoltage, exceeding the trigger voltage, the transistor goes into avalanche. For ordinary bipolar transistors, this is a failure mode and would possibly lead to destruction. Open-base technology based ESD protection devices are specifically designed to withstand ESD and surge pulses under these conditions. At the same time, they exhibit significantly lower parasitic capacitances than Zener diodes and a very low dynamic resistance. Because this is a single chip solution, the ESD proception devices can be integrated into very small packages allowing for miniaturization and maintaining signal integrity at high frequencies.

When the transistor structure goes into avalanche, a snap back of the voltage happens. Depending on the physical implementation, several snap backs can be observed. Depending on the desired application, these snap backs are tuned to behave as desired. Figure 26 shows the TLP curves of two open-base technology based ESD protections. The PESD2CANFD24V-T is designed to protect the CAN FD interface and the PESD24VF1BL is designed to protect antenna interfaces. As the CAN FD data line needs to survive 27 V DC, the snap back is only very small. The antenna interface is not exposed to such high DC voltage, so the device can have a larger snap back resulting is lower clamping voltages.

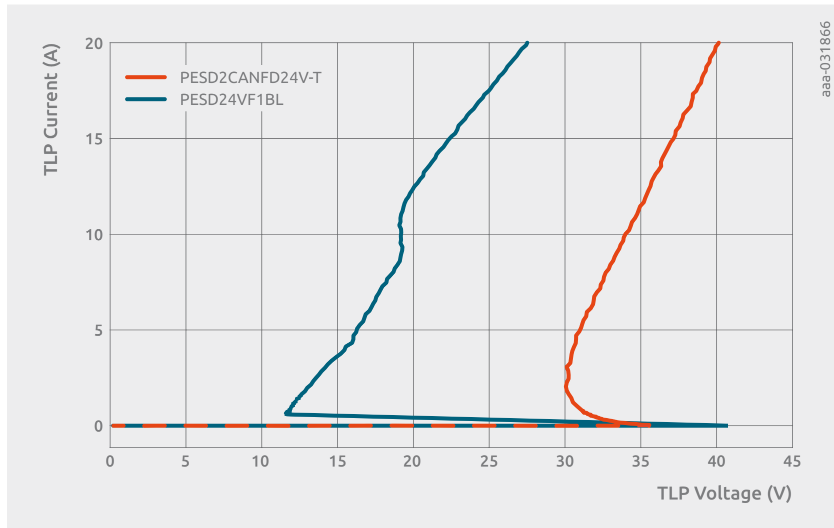


Figure 26 | TLP graph for positive pulse of open-base technology based ESD protections: PESD2CANFD24V-T and PESD24VF1BL

There is no common circuit symbol for open-base technology based ESD protection devices. Usually, two back to back cascaded diode symbols are used to illustrate the bidirectional behavior.

4.5 Rail-to-rail topology with SCR

Figure 27 contains a modification of the conventional rail-to-rail topology. Instead of a Zener diode, an silicon-controlled rectifier (SCR) is put between upper rail and ground. If the voltage of the upper rail exceeds a specified trigger voltage, the SCR switches into on-state and connects the two rails. If the current through SCR falls below a specified hold current, the SCR switches off again and becomes high-ohmic again.

Please note that when this protection topology is used, a supply line cannot be connected to the upper rail or to the signal inputs. In the case of a trigger event, the SCR would not return into the off-state because a DC-supply can easily provide a constant current above the hold current I_{hold}. The ESD protection component could be damaged or the supply line stays in a short-circuit condition. Therefore, in automotive, SCR technology is only used to protect multimedia interfaces and SerDes interfaces, when there is no risk of short-to-battery events.

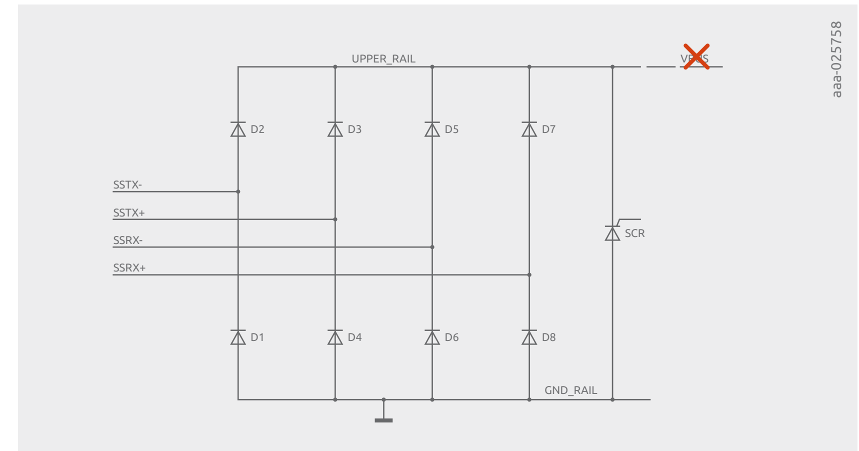


Figure 27 | Rail-to-Rail ESD protection device with SCR

The advantage of the SCR-based approach is that very low clamping voltages can be achieved for surge events. The turn-on effect is often called snap-back because the voltage at the ESD protection device jumps down from a trigger voltage towards a low voltage in on-state. The snap-back voltage can be designed to drop lower than the high state voltage of a signal line and below V_{RWM}. Although this appears to be a conflict, in most cases it does not create a problem. Many high-speed interfaces are designed to be free of DC content in the data stream. Therefore, the data lines do not stay in single-ended high-state. Once the signal toggles back to low-state the hold current or hold voltage condition for the SCR is violated and the ESD component switches off again.

Beside testing with a suitable I-V curve tracer, the snap-back characteristic can best be evaluated with a TLP test. Figure 28 shows a TLP curve of PESD3V3Z1BSF as an example for a TrEOS snap-back device. The device triggers at about 9 V and snaps back to 2.5 V. From there the TLP I-V-graph shows a mostly linear curve with a steepness of $R_{dyn} = 0.19\,\Omega$.

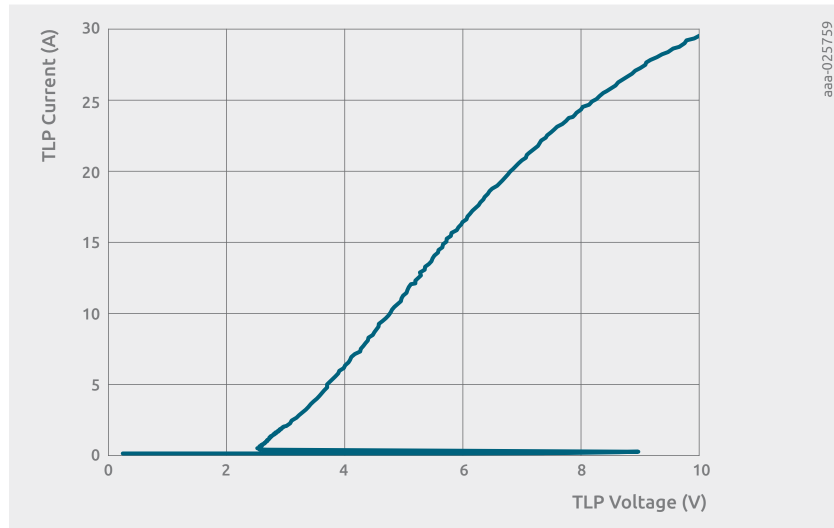


Figure 28 | TLP-Curve example of PESD3V3Z1BSF

Figure 29 compares typical TLP curves with each other, as described below.

- **Green TLP curve:** ESD protection products that are based on an avalanche effect clamping topology that are specified for operating with V_{RWM} 5 V to 5.5 V. They have a breakdown voltage V_{BR} that is equal to or greater than 7 V.
- **Red TLP curve:** Parts that are specified for operating below or equal V_{RWM} 3.3 V have a lower breakdown voltage of typically equal or greater than 5 V. Thus, clamping voltages are lower and more current of the surge event is dissipated in the protection device compared to the 5 V type.
- **Yellow TLP curve:** TLP testing can also be applied to interface pins and complete electronic products. Modern ICs often show TLP curves that start at relatively low voltages. As soon as the pulse voltage is raised, they show a steep increase of current, which is due to a low dynamic interface resistance.
  Please note that many ICs can only cope with a relatively low maximum TLP current. This can be $I_{PP} = 5$ A, for instance.

- **Black TLP curve:** Shows a deep snap-back topology example. By adding an SCR, very low clamping voltages after turn-on of the device can be realized. A big portion of the surge energy is dissipated in the ESD protection and the overall system level robustness is improved. The destruction voltage of the yellow curve is reached for much higher currents.

In conclusion, effective ESD protection requires a TLP curve for the ESD protection device that is located left of the TLP curve of the SoC. The curve must show a high steepness with no cross point to the SoC curve. In this way it can be ensured that most of the surge current flows through the protection; and only a lower current through the IC input structure. The point where the system is destroyed is shifted to higher currents. An ideal TLP curve would be perpendicular ($R_{dyn} = 0\,\Omega$), where the clamping voltage does not increase with the surge current.

With an avalanche topology, the breakdown voltage cannot be decreased any further down into the operating voltage range of the interface without causing leakages. This means that further improvement for a low clamping voltage can be driven in the direction of a perpendicular TLP curve only. However, dynamic resistance decrease has technological limits. Therefore snap-back topology allows lowest clamping voltages and highest system protection levels for sensitive interfaces.

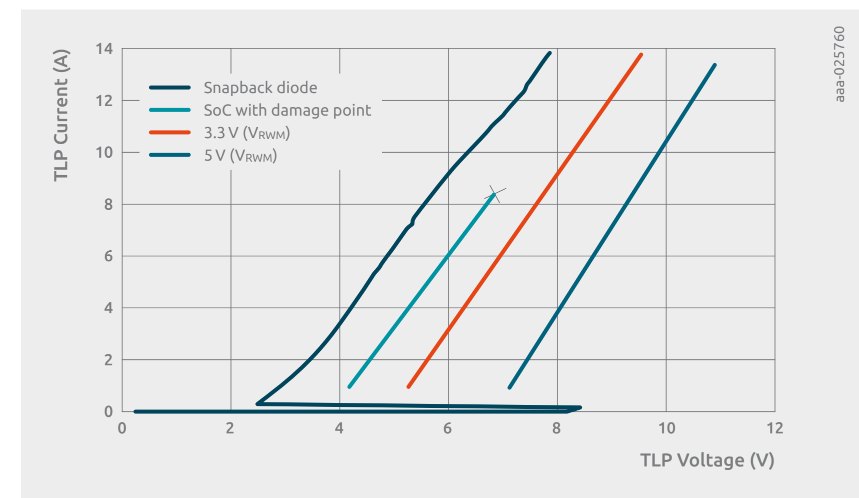


Figure 29 | TLP-Curves of avalanche type ESD diodes with V_{RWM} 5 V (green), V_{RWM} 3.3 V (red), SoC (yellow with point of destruction) and snap-back ESD diode

4.5.1 Latch-up scenarios

If a snap-back device is triggered, a latch-up can happen if the on-state current is higher than the hold current of the ESD protection device. However, most ESD protection devices withstand the current arising from this condition: Nexperia parts were tested in latch-up with 100 mA for several hours without showing any damage or degradation. If an interface is affected, a soft fail occurs but no hardware fail. For many interfaces, the snap-back device automatically returns to its off-state once the affected data line is in single-ended low state.

In automotive context it is important to mention, that latch-up scenarios associated with short-to-battery events need to be considered. If short-to-battery events have to be withstand, like for CAN FD, SCRs are not applicable. For automotive Ethernet, short-to-battery is considered as well. Therefore, SCRs are not suitable to be placed at the connector. However, they suitable to be placed directly at the PHY as there is a DC decoupling in-between.

An HDMI interface requires some attention with respect to possible latch-up conditions. The HDMI interface topology is given in Figure 88. Many HDMI input circuits are designed with active silicon circuits for the 50 Ω pull-up resistors. HDMI interfaces have to be safe for short-circuits on the TMDS lines according to HDMI standard requirements. To avoid overheating of active pull-up resistors, the pull-up voltage is shortly removed whenever a short is detected at the TMDS lines. This mechanism releases a latch-up condition.

Please note that Transmission Minimized Differential Signal (TMDS) lines begin data transfer after connection is established. The risk of ESD strikes is much higher during the connecting process of a cable, and very unlikely to happen at a cable with fully established connection. In practice, no known field returns are caused by latch-up failures with HDMI interfaces.

The maximum latch-up current for HDMI can be calculated in a straightforward way. The pull-up voltage can be 3.5 V (3.3 V + 5%) as maximum and the pull-up resistors can have a minimum resistance of 45 Ω (50 Ω −10%). Assuming a snap-back voltage of 1.24 V, the maximum potential latch-up current can be calculated as 50 mA. If the hold current of the ESD protection is smaller than this value, there is a potential risk for the interface to hang-up. More Details on HDMI interfaces can be found in Section 9.2.

I²C bus interface is another example that can be affected by latch-up conditions. The maximum high-state current of this interface is defined by the selected pull-up resistors. There is no potential problem if the high-state current is lower than the hold current of the ESD protection device. If it is higher, the I²C-bus master detects the hang-up situation on the bus and can initiate a power cycle to release the bus again.

4.5.2 Analyzing load lines to judge the risk of latch-up scenarios

Figure 30 shows an I-V characteristic of an interface output driver with a detailed I-V diagram of a snap-back ESD device.

The load line of an interface starts at a short circuit current on the y-axis. It shows a linear decay toward the open circuit case where the x-axis is crossed at the data line drive voltage V_{DD}.

The ESD protection I-V curve shows a hysteresis. The arrows mark which trace is valid for the direction of test voltage change. If the voltage increases, the snap-back triggers as soon as the trigger voltage is reached. From that point onwards, the curve continues on a steep on-state path. When the testing current is decreased below I_{hold}, the ESD protection device turns off again, utilizing the lower paths, shown in the diagram, to leap to higher voltage. In similar scenarios as shown in the diagram, an ESD strike can produce a latch-up condition. An interface can get stuck at operating point 1. To be safe from a latch-up scenario, the load line of an interface should only cross the I-V curve of the protection device once.

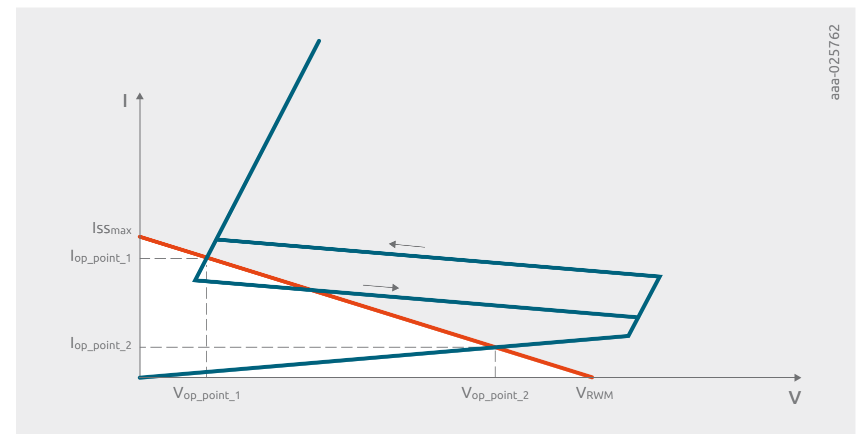


Figure 30 | I-V characteristic of interface output driver (red) and snap-back ESD protection device (blue)

In an established USB Type-C connection (pin assignment Table 21), the configuration channels CC1 or CC2 are connected to V_{conn}. V_{conn} is a 5 V DC supply. Sideband usage signals SBU1 and SBU2 can be overlaid by a DC. This applies to analog audio use cases in which the DC supplies amplifiers. A snap-back ESD diode that can snap below a DC level of a signal line should not be selected for these cases. Of course, V_{Bus} is not suitable for snap-back devices in this context.

4.5.3 Hold current and hold voltage of TrEOS protection devices

In Figure 31 the I-V curve shows measurement results with a current-driven curve tracer for the unidirectional TrEOS product PESD4USB5U-TBR. The curve delivers a hold current of I_{hold} 18 mA and a hold voltage of V_{hold} 1.5 V. A hysteresis curve can be seen, as explained in the previous section. I_{hold} and V_{hold} can be derived from the current and voltage point at the lower left corner of the hysteresis area.

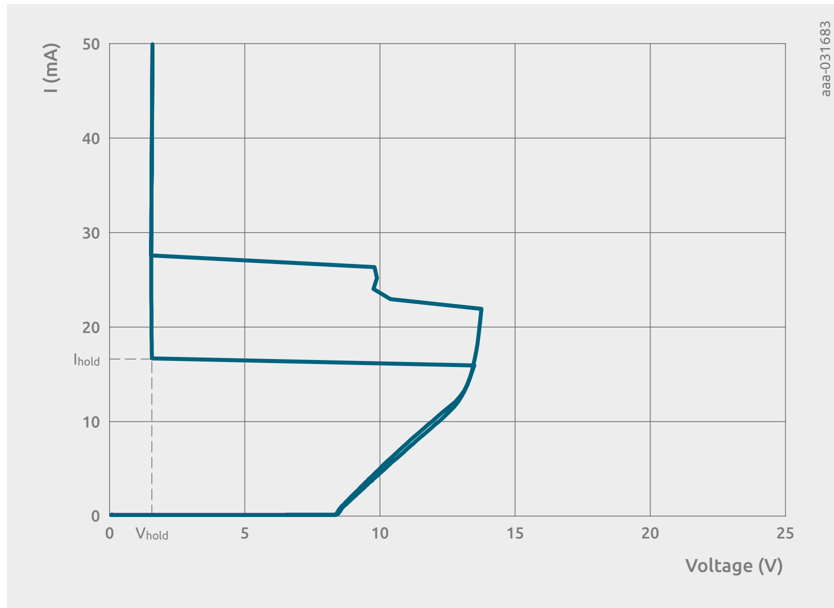


Figure 31 | I-V curve of unidirectional PESD4USB5U-TBR with hysteresis characteristic

The I-V curve of Figure 32 shows measurement results with a current-driven curve tracer for the bidirectional TrEOS product PESD4USB5B-TBR. The curve delivers the same hold current as for the unidirectional part, which is I_{hold} +/– 15 mA. The hold voltage is $\pm V_{hold}$ 2.3 V. The hold voltage V_H is higher because of the bidirectional solution's series structure, which also includes an additional V_F value of 0.8 V of a diode that is driven in forward direction.

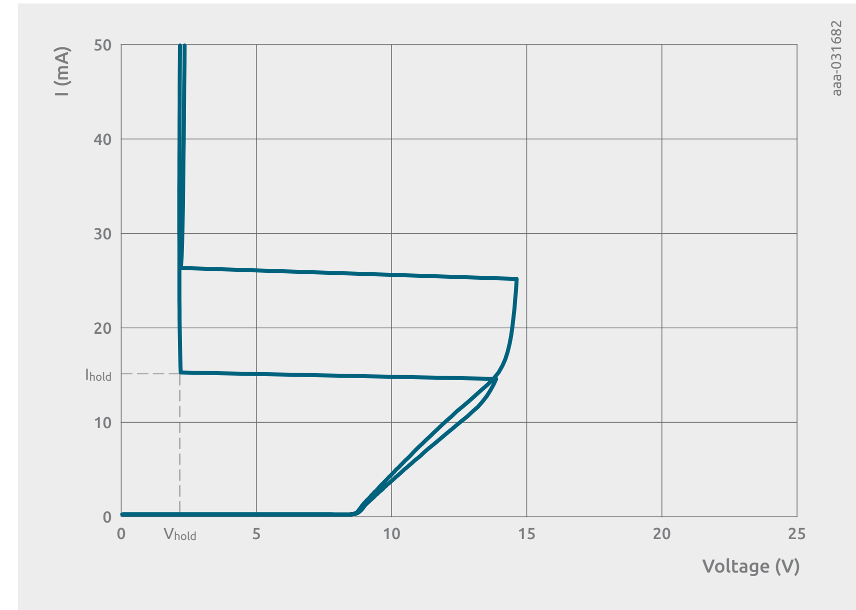


Figure 32 | I-V curve of bidirectional PESD4USB5B-TBR with hysteresis characteristic

4.5.4 Switching speed of snap-back ESD protection

An effective ESD protection limits a surge pulse to a safe clamped voltage within a short time without excessive and wide overshoots. This temporal behavior, as shown in Figure 33, can be evaluated with a VF-TLP test by analyzing the voltage traces of the single test events.

Figure 33 shows a voltage and current trace of a VF-TLP test for a PESD4USB5U-TBR at a peak current I_{PP} of 15 A, with pulse width 5 ns, and rise and fall time of 600 ps. The voltage trace shows a narrow overshoot. After device turn-on, the comparatively low clamping voltage is reached [14].

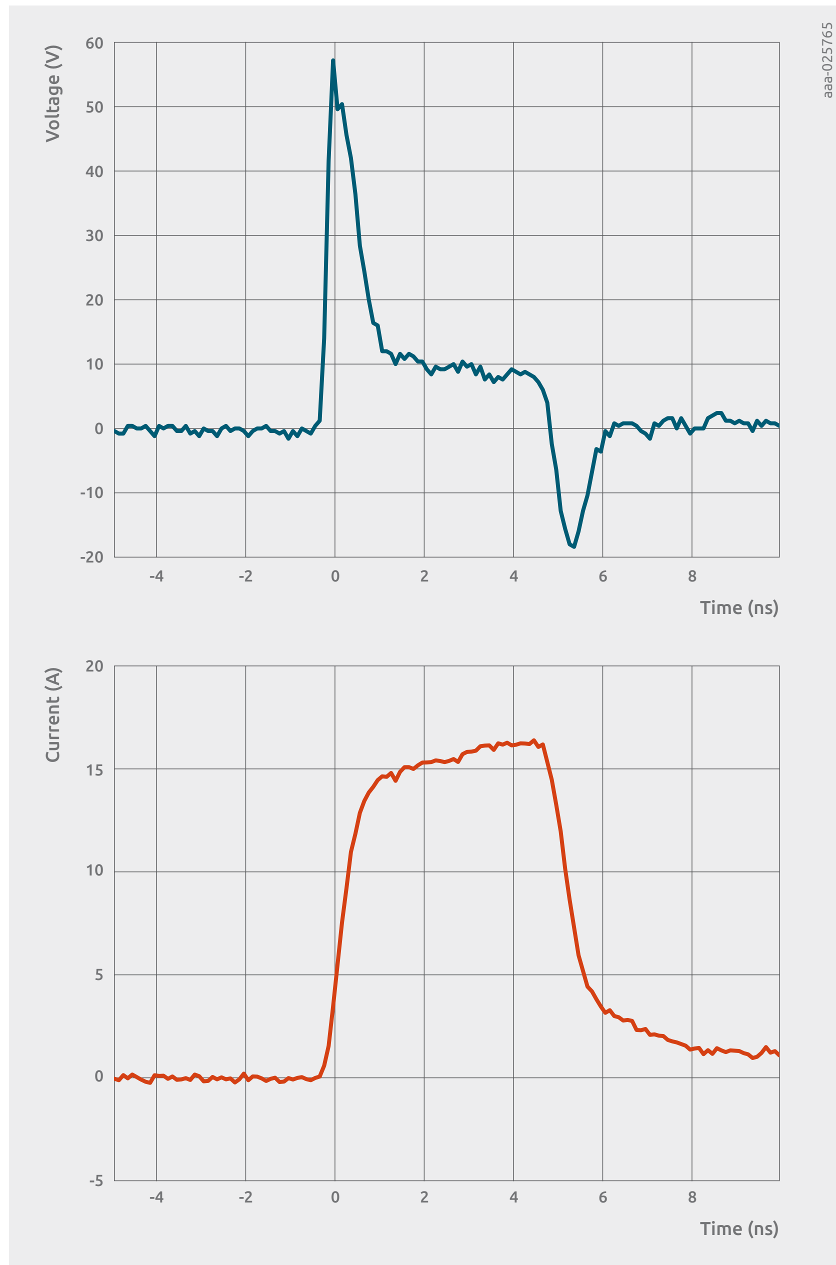


Figure 33 | VF-TLP (5 ns/200 ps) voltage and current traces PESD3V3Z1BSF at I_{PP} = 15 A

Figure 34 shows a way how the turn-on time can be derived from a VF-TLP voltage scope trace. The average value in the 70% to 90% window is taken as zero percent reference value for the falling edge. The TrEOS devices turns on within approximately 1 ns, as Figure 33 shows. The switching time interval is derived from the 30% values at the rising and falling edges of the voltage overshoot in the scope trace.

For many products in the market, the turn-on time is relatively long. This prevents the device from switching on at all in a VF-TLP pulse. Turn-on times of about 10 ns are often encountered. Devices that show this weakness cannot protect very sensitive high-speed interfaces and cannot achieve the required system robustness.

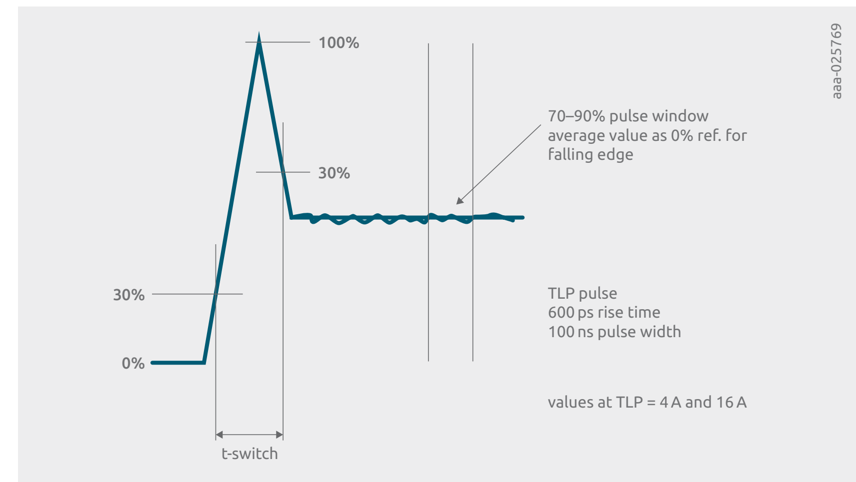


Figure 34 | Measurement of switching time (turn-on time) based on VF-TLP test pulse

4.6 Footprint comparison

For signal integrity, the routing is a crucial point. Even though, the parasitic capacitance deteriorates the signal quality, at very low capacitances, the routing that is done to connect the package plays an important role. In this section, a few different ways to route common automotive packages are compared. The most important general finding complies with best practice signal integrity design: avoid switching layers, avoid using stubs. The following measurements are conducted with a VNA[1]. The system was calibrated to the probe tip, so the traces before and after the footprint are not de-embedded. The parameters shown are differential insertion loss (S_{21dd}), return loss (S_{11dd}), and differential to common mode conversion (S_{21dc}). In the following plots, the dashed lines refers to the case of straight traces without a footprint.

4.6.1 Leaded 3-pin packages: SOT23

The industry standard SOT23 was introduces in 1969 by Phillips and is today the most common package for ESD protection devices by all vendors. The, for todays standards, relatively big size of the package requires to open the differential signal trace or to tilt the footprint. Figure 35, shows the common way of connecting the package (A), and tilted versions (B) and (C). Figure 36 shows the insertion loss, return loss and differential to common mode conversion.

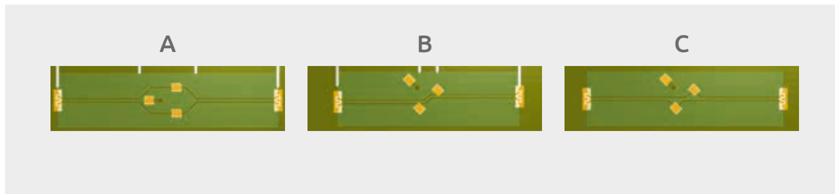


Figure 35 | Common routings for external ESD protection devices in SOT23

1 Rohde & Schwarz ZVA40

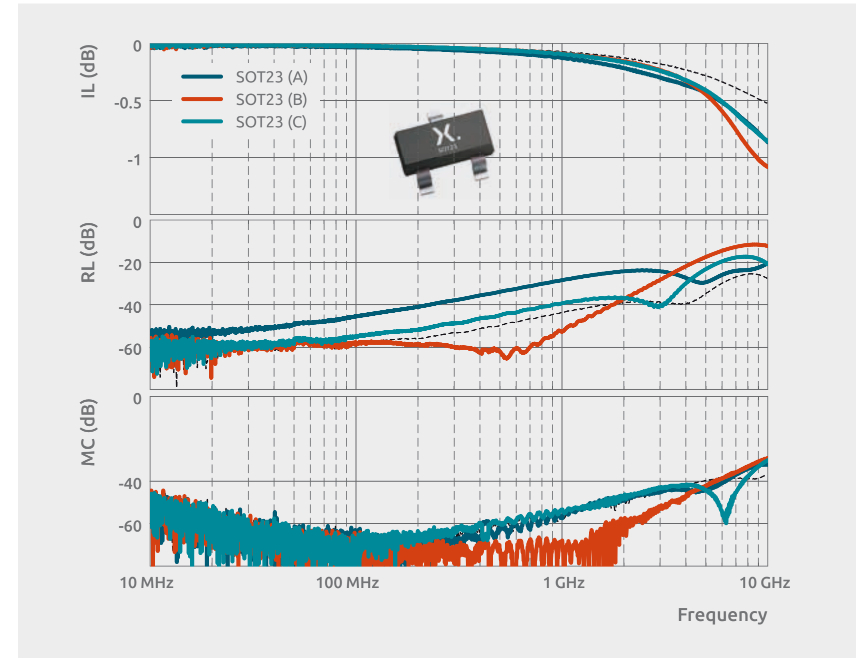


Figure 36 | Insertion loss (IL), return loss (RL), and differential to common mode conversion (MC) for the design shown in Figure 35

Generally, the differences are not very big. Version A shows more return loss at low frequencies that the tilted versions. Version B performs very well at lower frequencies but is performing worth at higher frequencies. Version C is performing best overall frequencies. If routing guidelines allow for version C, it should be considered in case of signal integrity concerns. For interfaces where frequencies above 3 GHz are irrelevant, all variants are ok.

4.6.2 Leaded 6-pin packages: SOT363

Leaded 6-pin packages are popular for many interfaces and are often used to protect two lines. Usually, the ground pin is located in the middle and the standard way of routing illustrated in Figure 37 (A). To avoid opening the traces, a version with small stubs (B) is also promoted sometimes. Ground-to-any devices or special configurations also allow to connect the ground pin at the side (C) in some cases.

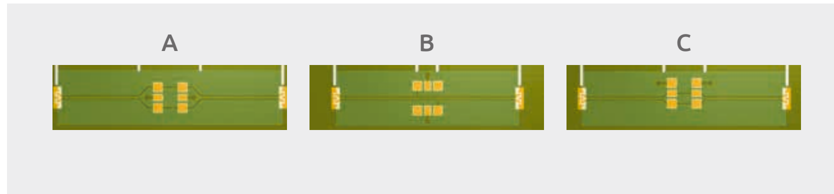


Figure 37 | Common routings for external ESD protection devices in leaded 6-pin package SOT363

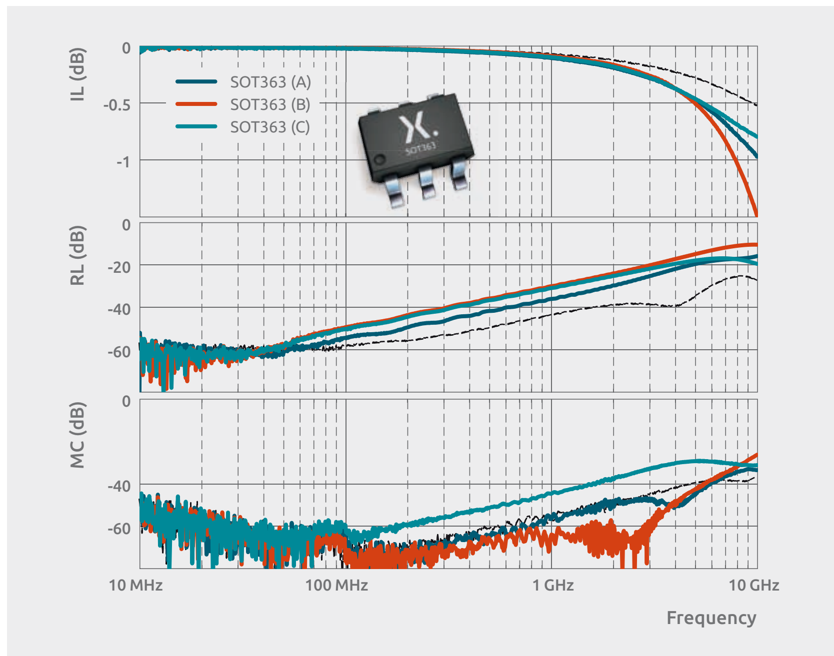


Figure 38 | Insertion loss (IL), return loss (RL), and differential to common mode conversion (MC) for the design shown in Figure 37

Looking at the RF-Characteristics in Figure 38, the standard configuration (A) performs best. Version (C) provides slightly improved transmission, at the cost of increased return loss and significantly increased mode conversion. Version (B) with the stubs, improves the mode conversion for higher frequencies, but performs worth in terms of insertion and return loss.

4.6.3 Leadless 3-pin packages: DFN1110-3

Leadless packages are getting more popular also in the automotive domain. A 3-pin package that is also used to house transistors and switching diodes has a heatsink that needs to be circumvented by the traces, see Figure 39 (A). Alternatively, if the PCB design allows, the device can be placed on the opposite side (B). This allows to keep the routing nearly unchanged. However, the vias form subs.

Figure 39 | Common routings for external ESD protection devices in leadless 3-pin package DFN1110D-3

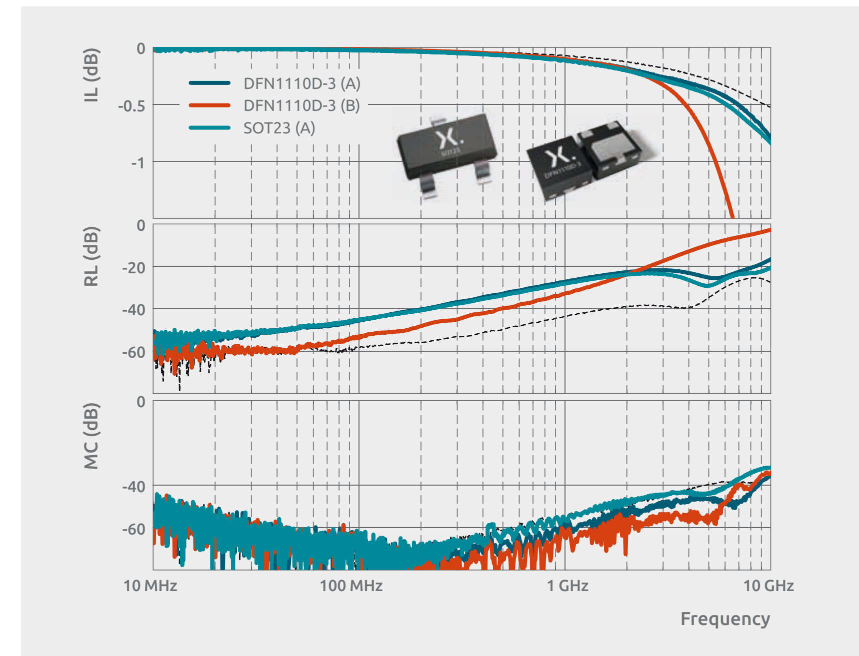


Figure 40 | Insertion loss (IL), return loss (RL), and differential to common mode conversion (MC) for the designs shown with DFN1110D-3 in Figure 39. and SOT23 in Figure 35

As seen in Figure 40, Version B, where the protection device is located on the opposite side of the PCB should be avoided. Despite the stubs that are introduced by the vias, the pads form parasitic slot antennas decreasing the performance especially at high frequencies. The standard routing version A performs like a good SOT23 implementation. The increase of the return loss depends on the proximity of the traces to the ground pad.

Please note, that here empty landing pads are compared. In real protection devices, additional parasitics of the package come on top. Leaded packages have higher parasitic inductance and capacitance decreasing the over all performance. Figure 41 shows the same routing schemes with a PESD2CANFD24V-T for SOT23 and PESD2CANFD24V-QB for DFN1110D-3. It is seen that the very similar performance of the empty footprints starts to deviate when devices are mounted. Here, both devices have the same diode capacitance of 5.3 pF. However, the leads of the SOT23 package appear as stubs and the larger metallic structure inside the package adds additional parasitics.

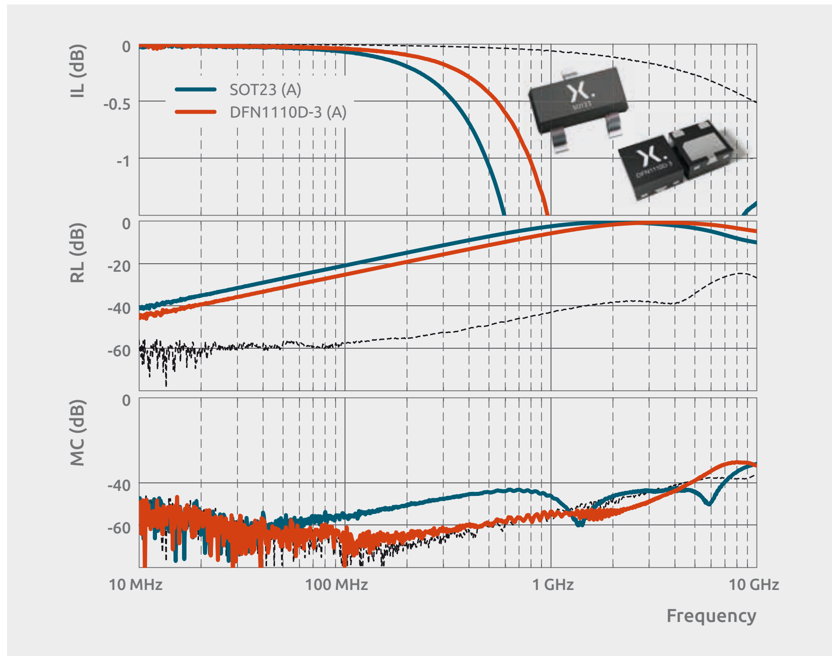


Figure 41 | Insertion loss (IL), return loss (RL), and differential to common mode conversion (MC) for the designs shown with DFN1110D-3 in Figure 39 mounted with a PESD2CANFD24V-QB and SOT23 in Figure 35 mounted with a PESD2CANFD24V-T

4.6.4 Leadless 2-pin package: DFN1006-2

Especially, in high-speed interfaces, leadless 2-pin packages are getting more popular. Due to their size, they allow for miniaturization compared to leaded 3-pin packages and at the same time can be used very flexible in the existing routing. Figure 42 shows two typical routing schemes. In practice, many more variants are possible, as it is possible to get very close to the connector or to integrate the devices in existing termination networks.

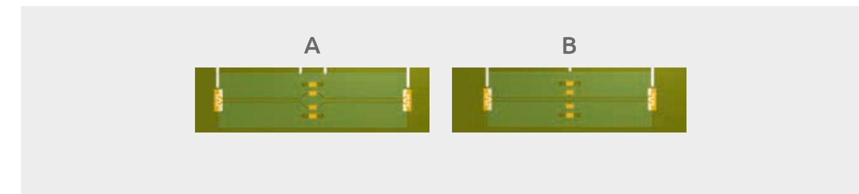


Figure 42 | Common routings for external ESD protection devices in leadless 2-pin package DFN1006D-2

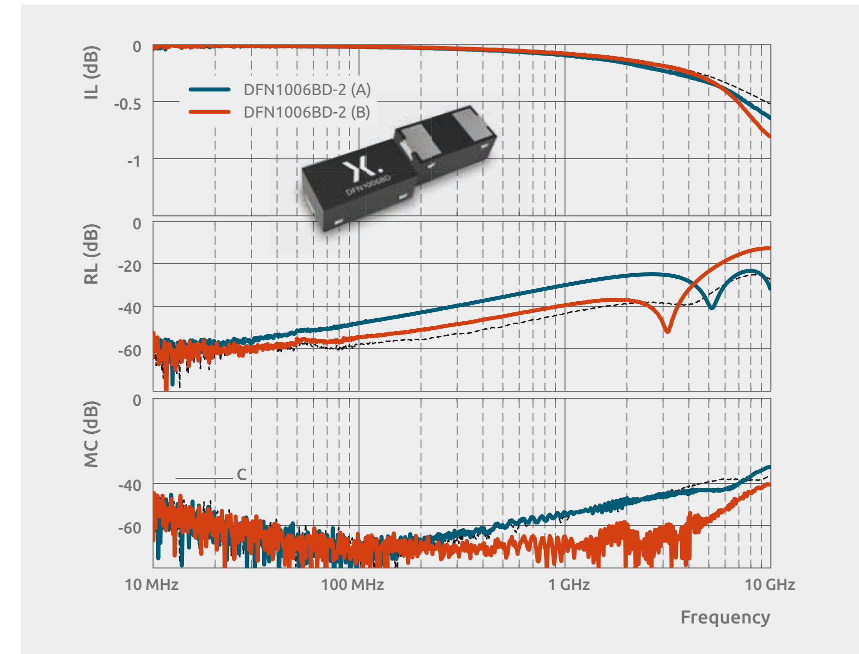


Figure 43 | Insertion loss (IL), return loss (RL), and differential to common mode conversion (MC) for the designs shown with DFN1006D-2 in Figure 42

Figure 43 shows the corresponding RF characteristics of the two layouts. It is generally seen that the insertion loss can be improved. However, the return loss and mode conversion highly depend on the actual routing and should be optimized for every individual application if required.

Chapter 5

Failure symptoms in electronic components caused by ESD and surge events

In case electronic devices have been destroyed, silicon chips or electronic components are often analyzed if visible failure symptoms like burn marks can be found. The nature of the destructive event shall be found out from such inspection. It shall be concluded if damage was caused by an ESD strike , by a more massive surge event or by excessive thermal stress above the specified limits. For this kind of classification it is worthwhile to have a brief comparison of most important key parameters of standardized surge signals.

Table 10 lists these key parameters of different surge testing standards in a direct comparison. IEC 61000-4-2 events have a very short rise time, peak current is high with 30 A for an 8 kV ESD gun strike. Anyhow pulse energy is not very high with about 16 µJoule. Human Body Model (HBM) [15] pulses carry even less energy and show lower peak current and slower rise time. 8/20 µs test pulses have about 3 decades more energy compared because of the long pulse duration and low surge generator output resistance. 100 ns TLP pulses are in a similar league in terms of pulse energy and rise times like IEC 61000-4-2 pulses, whereas very fast TLP is even lower in energy. A pulse with a peak current of 15 A corresponds to about 3.5 mJoule.

Figure 44 shows a good example of ESD damage at an IC die. The damaged area is very small, nonetheless insulating layers and gate oxide can be degraded and destroyed. Leakage current can lead to functional fail. Figure 45 gives another example of ESD damage. It shows a tiny hole burnt into the crystal as a visible result of the surge event.

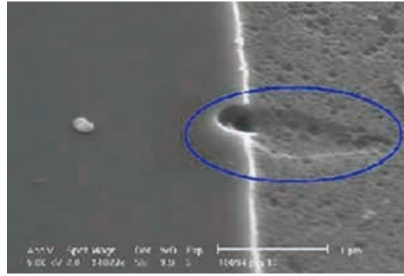


Figure 44 | ESD damage with small burn mark

Figure 45 | Example of ESD damage

Table 10: Comparison of surge standards

Parameter	8kV System level ESD (IEC 61000-4-2) [6]	8kV Chip level ESD HBM (JESD22-A-J114D) [15]	Short Circuit Surge (8/20µs) (IEC 61000-4-5) [5]	TLP [11,12]	Very fast TLP (VF-TLP) [13]
Rise time	1 ns	10 ns	8 µs	1 ns	300 ps
Pulse length	not specified (>100 ns)	not specified (>400 ns)	28 µs	100 ns	5 ns
Peak current	~30 A @8 kV (1 ns) ~16 A @8 kV (30 ns)	~6 A @ 8 kV (10 ns) ~2.2 A @ 8 kV (160 ns)	up to 2000 A	up to 80 A	up to 80 A
Peak Power	~3000 W (30A,100 V)	~120 W (6A,20 V)	~250 W (15 A,16 V)	~200 W (25 A, 8 V)	~200 W (25 A, 8 V)
Average Power	~160 W (16 A,10 V)	~22 W (2.2 A,10 V)	~125 W (7.5 A,16 V)	~200 W (25 A, 8 V)	~200 W (25 A, 8 V)
Pulse Energy	**~16 µJoule**	~8.8 µJoule	**~3.5 mJoule**	~20 µJoule	~1 µJoule
Pulse Shape	I_{peak}, Time	I_{peak}, Time	I_{peak}, Time	Current (A), Current (CH-2), Time (ns)	

The damage shown in Figure 46 shows a burn mark created by an IEC 61000-4-5 robustness test. The die of a logic buffer was exposed to an 8/20 µs surge pulse from a generator programmed to 42 V charging voltage. The peak current of this test can be assumed to be roughly 20 A with the 2 Ω output resistance of the generator used. The burned area is bigger compared to an ESD strike; metal connections are fully burnt away.

Figure 47 is an example of an EOS (Electrical Overstress Event). Such damage results from thermal overstress where limiting values for power dissipation or maximum current of a device have not been obeyed. The damages on the crystal are severe and the burnt area is relatively big. Sometimes packages are cracked and carbonized with EOS damages. In the case of high currents, fused bond wires are very often observed.

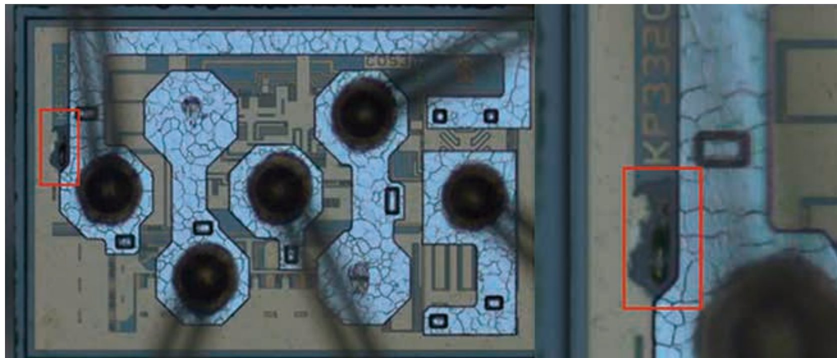


Figure 46 | IEC 61000-4-5 surge pulse damage (8/20 µs surge with 42 V generator set-up)

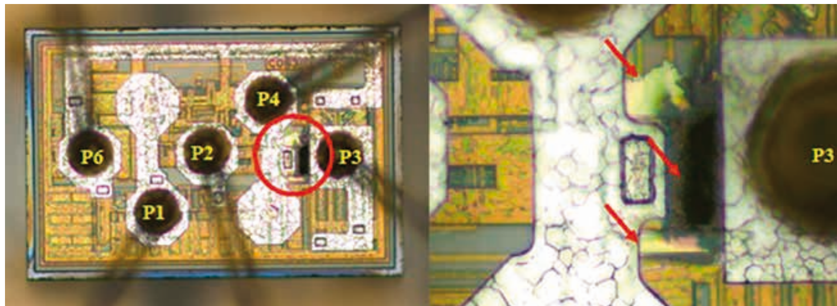


Figure 47 | Electrical overstress damage example (EOS)

Chapter 6

Classical In-Vehicle Networks (IVN)

In-vehicle networks (IVNs) consist of multiple microprocessors communicating over different networks. They help manage entertainment and navigation functions or body, motor and safety control as well as lighting and other vehicle systems. A typical IVN topology is shown in Figure 48. This is called domain architecture as different functional domains are directly connected and interface with each other via a domain controller or gateway.

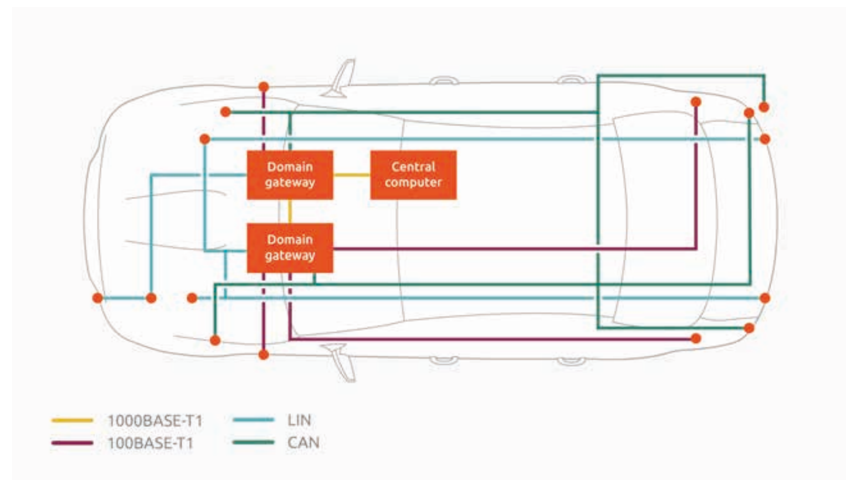


Figure 48 | Domain architecture of a classical in-vehicle network topology

A modern car contains up to 100 ECUs. To exchange all the data between them, several highly reliable IVN protocols (CAN, LIN, FlexRay, Ethernet, etc.) have been designed that can handle the car's physically challenging environment. To ensure safe operation, solutions are required to pass emission and immunity tests, and guarantee signal integrity. In this section, we will discuss LIN, CAN, and FlexRay as the most important interfaces in a classical IVN architecture. Ethernet will be discussed in the context of zonal architectures.

ESD protection diodes for automotive networks must conform with different electrical requirements to those typically found in smartphones or computers. First, ESD diodes need to protect the network and the transceiver pins against ESD strikes. Additionally, the ESD diodes themselves need to be safe against short-to-battery voltages and ensure that communication is not disturbed when the system is tested against electromagnetic interference (EMI). Diode capacitances need a certain matching in differential communication systems and the value of the capacitance needs to be low enough to maintain signal integrity. ESD protection diodes represent a capacitive load on the bus lines, which in differential systems can cause unwanted skew and jitter when not matched properly.

6.1 LIN interface

The first Local Interconnect Network (LIN) specification was published in 2003 by the LIN consortium, which concluded its work with the finalization of the LIN Specification 2.2.A in 2010. Conformance test specifications are now part of the ISO17987:2016 [16] and the latest revision of SAE J2602 [17]. This is a subset of specifications taken from the LIN Specification 2.0.

LIN is a concept for low cost automotive networks. It is typically used where the higher data rates and versatility of the CAN network is not required. It connects modules into a sub-bus that is connected to the existing CAN network. Typical modules where LIN is used are seats, locks, mirrors, or as interface to sensors, for example rain detectors. It uses a single wire, serial communication protocol and operates at low speed, with a maximum data speed of 20 kbit/s. The bus voltage level is approximately the supply voltage, in 12 V board net typically 14.4 V.

6.1.1 ESD protection devices for LIN

External ESD protection on the LIN bus connection is recommended by LIN transceiver suppliers for extending the ESD voltage level the module can withstand. Relevant electrical parameters for selecting external ESD protection diodes include the diode's breakdown and working voltages, V_{BR}, V_{RWM}, and capacitance C_d. Additionally, car OEMs have different requirements and guidelines. The generic interface design and positioning of the external ESD protection is shown in Figure 49. If other passives, like inductors or ferrites are present, the ESD protection should always be placed directly at the connector.

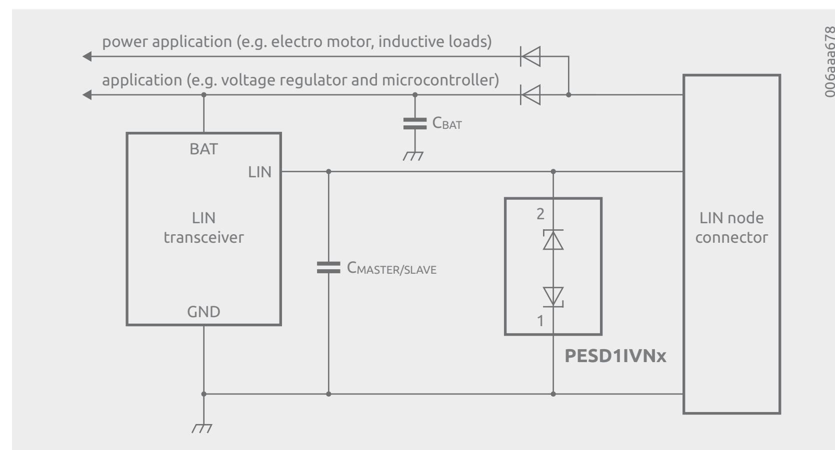


Figure 49 | Generic interface design of a LIN node with external ESD protection device

In addition, ESD protection diodes should be chosen to withstand the maximum battery voltage without being damaged, in case the LIN bus line is shorted to the battery line. For a 12 V board net the maximum battery voltage is 16 V. The operating voltage range for an ECU is defined between 8 V and 18 V, referenced to the local ECU ground. From this range definition, V_{RWM} should be bigger than 18 V. Typically, bi-directional ESD diodes are used for LIN bus application with a breakdown voltage bigger than +/– 27 V because of the following aspects.

Generally, the diode capacitance C_d has to be smaller than 100 pF to maintain signal integrity at the maximum data rate of 20 kbit/s. However, some car OEMs have different general or project-based requirements. Some OEMs do not specify a maximum capacitance for the diode, but for the complete link, so that the combination of external ESD protection, input capacitance of the transceiver, and the master/slave capacitor need be taken into account. To minimize the total impact of the diode on the system, C_d should be smaller than 30 pF.

6.1.2 Compliance testing

Compliance to the LIN specification [16] is tested together with a transceiver in a small reference system of three LIN transceivers, where one is protected by the ESD protection device under test. Therefore, these tests are sometimes called *combination tests*. Many car OEMs require Tier1 to have the combination to be tested before implementing it into a module. The compliance test consist of four different measurements: RF emission, RF immunity, immunity to transients, and ESD. In [16] the test conditions are defined, limits are set by the system owners — car OEMs.

For the emission test, the dummy network consists of the three transceivers, where one is protected by the device under test is communicating with arbitrary data. Additionally, every LIN node has a external capacitor of 68 pF attached to the LIN port. The setup is built on a single PCB to exclude the effect of long or open cables. The emitted energy is measured via capacitive coupling. From experience, this test is usually straightforward for a suitable ESD protection device. Figure 50 shows a typical measurement result.

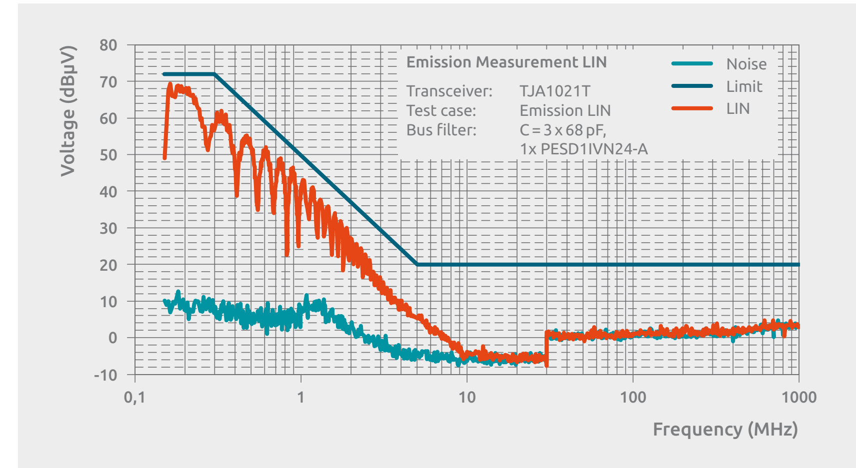


Figure 50 | Typical result (PESD1IVN24-A ESD protection with NXP TJA1021T transceiver) of emission measurement for [16] compliance

The test for immunity against RF disturbances is conducted on the same dummy network as used for the emission test and referred to as direct power injection (DPI) test. The RF disturbances are coupled via capacitors into the dummy network. The system is tested while communicating, which shall continue during the test, and sleep mode, where the transceivers should not wake up. Meanwhile the system is stressed with 36 dBm at frequencies from 1 MHz to 1 GHz using continuous wave modulation (CW). During the test, the power is monitored to ensure that there is not too much power absorbed by the system. Figure 51 shows a typical test result for the sleep mode.

When voltage amplitudes exceed the breakdown or trigger voltage of the ESD protection under test, it becomes conductive and power is absorbed by the system. This can lead to failing the test limits and occasionally the destruction of the ESD protection device. The higher the breakdown voltage, the less the system is affected. With diodes having a $V_{BR} \geq 27$ V, modern transceiver modules usually pass typical EMC tests as required by the automotive industry. To avoid impacting the module's EMC performance, it can be stated that the higher the breakdown voltage the better. However, to effectively protect against ESD, a low clamping voltage hast to be achieved. Therefore, a low dynamic resistance of the ESD protection device is the best way for a well-protected and EMC compliant system.

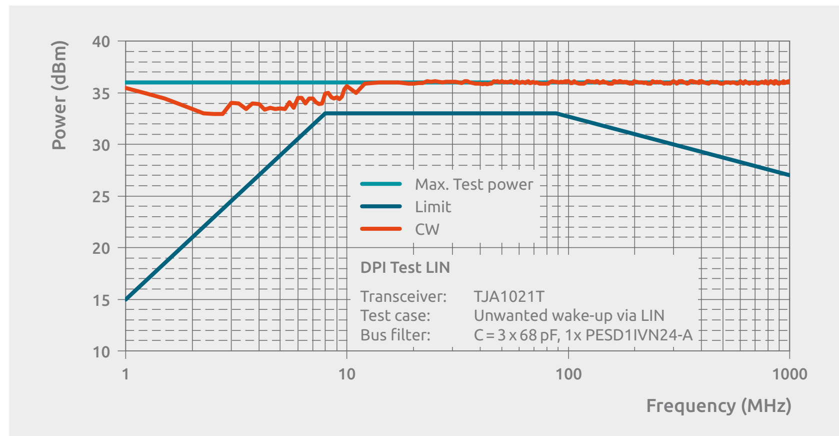


Figure 51 | Typical result (PESD1IVN24-A ESD protection with NXP TJA1021T transceiver) of immunity against RF disturbance measurement for [16] compliance

Besides RF immunity, immunity against transients is tested. Again, it is tested during communication and in sleep mode. Also, the same dummy network is used and the pulses are coupled capacitively. The test pulses are Pulse 1, 2a, 3a, and 3b from ISO7637-2 [9]. The pulses are described in more detail in Section 3.5.

Finally, the actual robustness against ESD is tested. There are two tests for robustness against ESD. Both use a dummy system with a single transceiver and a generator with an IEC 61000-4-2 compliant waveform. In one test, ESD is applied directly to the connector of the LIN interface. The second is a discharge into an attached cable. Functionality is tested via the I/V characteristic and a check of the send waveform. Modern ESD protection devices are able to achieve 30 kV robustness in both scenarios.

6.2 CAN interface

Developed in the 1980s by Robert Bosch GmbH, the Controller Area Network (CAN) specification became an ISO standard [18–22] in the early 1990s. CAN is a very well-established network for automotive and is considered faster and more flexible, but more expensive, than LIN. A CAN network typically uses a two wire, twisted pair cable to transmit and receive serial data. High-speed CAN (parts 2, 5, and 6 of the ISO11898), specifies transmission rates up to 1 Mbit/s. Low-speed, fault-tolerant CAN (part 3 of the ISO11898), specifies up to 125 kilobits per second.

Fault tolerant often means that the transceiver can switch from a differential receive and transmit capability to a single-wire transmitter and/or receiver in error conditions. This means single ended +12 V bus voltage max, and differential –12 V bus voltage maximum. Sometimes, single-wire CAN (SWCAN), specified in SAE J2411 [19], is used as an alternative for LIN. From an ESD perspective, external protection devices that are suitable for LIN, are usually suitable for SWCAN. However, there might be tighter requirements on the maximum allowed capacitance. A generic CAN interface is shown in Figure 52.

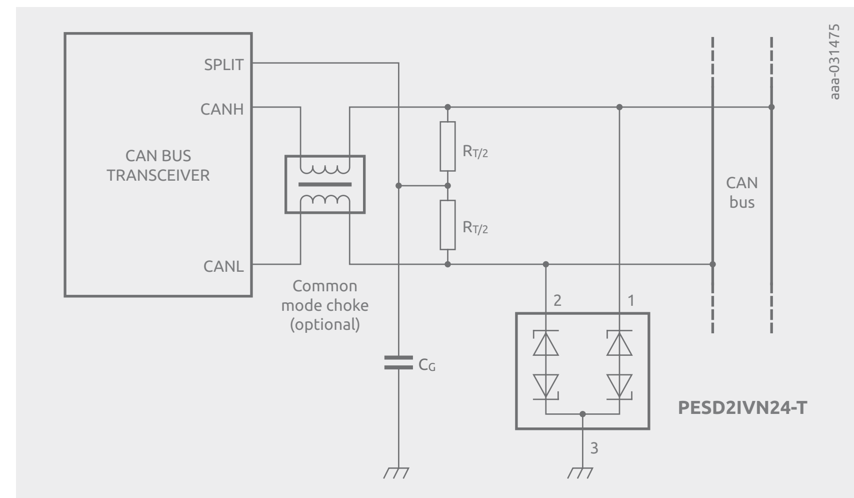


Figure 52 | Generic CAN interface

Figure 53 shows a CAN bus example with different node options. Node 1 shows a subsystem with microcontroller connected via a CAN controller and a CAN transceiver to the bus. For Node 2, a microcontroller with built-in CAN controller is used, whereas for Node N a CAN I/O Expander is attached to the bus providing extra I/Os, pulse width modulated outputs or analog/digital converter (ADC) inputs for general usage. Microcontrollers that fully integrate a CAN transceiver and CAN controller as shown in Node 3 are also available.

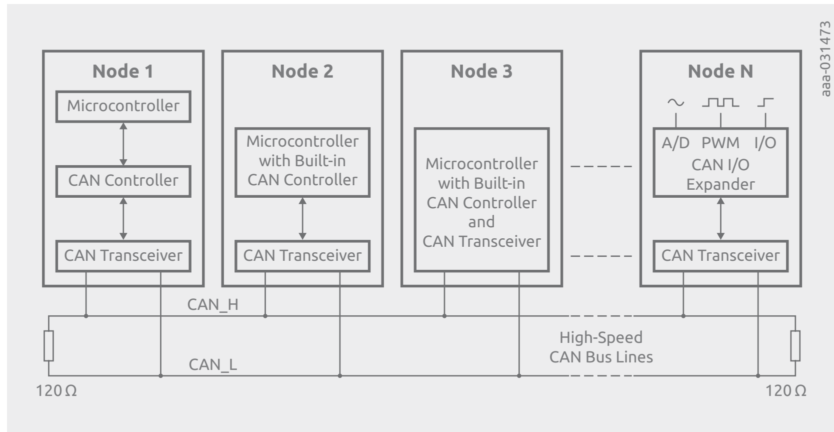


Figure 53 | CAN Node configurations

6.2.1. Low-speed CAN

A CAN transceiver provides the physical link between the protocol controller and the physical bus wires in a network. CAN_L is the LOW-level CAN bus line. In normal operating mode, the value of Dominant state is about 1.4 V and the value of Recessive state is 5 V. In low-power modes, the voltage of CAN_L is equal to the battery voltage. CAN_H is the HIGH-level CAN bus line. In a typical operating mode, the value of Dominant state is about 3.6 V and the value of Recessive state as well as in low-power modes is 0 V.

Figure 54 explains the CAN bus logical states Dominant and Recessive in low-speed mode. A Dominant state can overwrite a Recessive state. The Recessive state is the idle state of the interface and represents logical 1. In Recessive state, CAN_H has a nominal voltage of 0 V and CAN_L has a voltage of 5 V. The signal line CAN_H toggles between the single-ended low state voltage of 0 V and a high state voltage of 3.6 V. The CAN_L signal has a low level of 1.4 V and a high level of 5 V. So both lines have a nominal swing of 3.6 V. For the logic state, Dominant CAN_H is bigger than CAN_L for a differential receiver whereas in Recessive state CAN_H is lower than CAN_L.

Normally the CAN bus receivers exploit the differential voltage on the CAN lane. For low-speed the receivers can switch to a mode where data reception is based on a single line only. This is a fallback mode if one of the signal lines is broken. The single line mode is called Limp-Home-Mode.

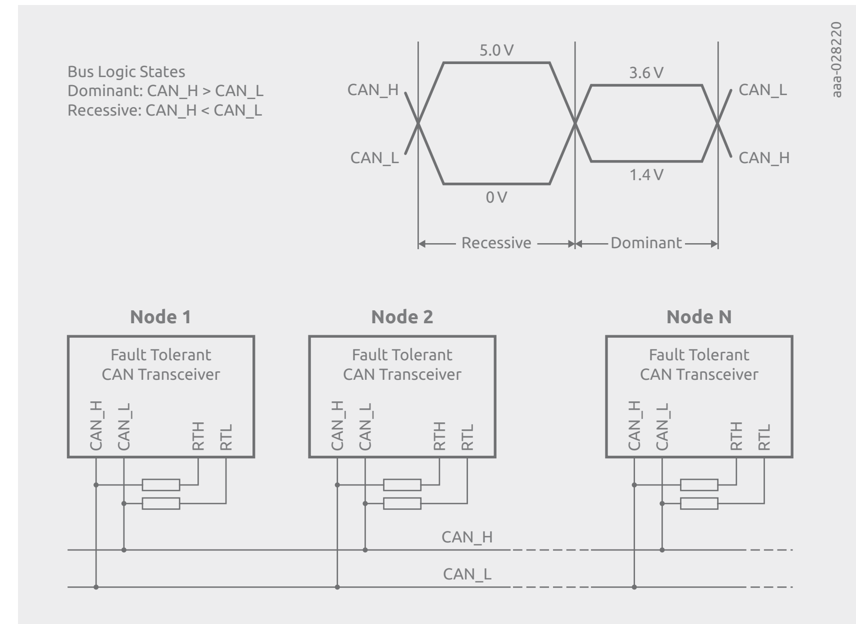


Figure 54 | Low speed CAN bus logical states

6.2.2 High-speed CAN

In Figure 55, the Highspeed CAN bus voltages are depicted. In idle state or Recessive state both signal lines have a voltage level of about 2.5 V. In Dominant state CAN_H jumps up to 3.5 V and CAN_L goes down to 1.5 V, creating a differential voltage of 2 V.

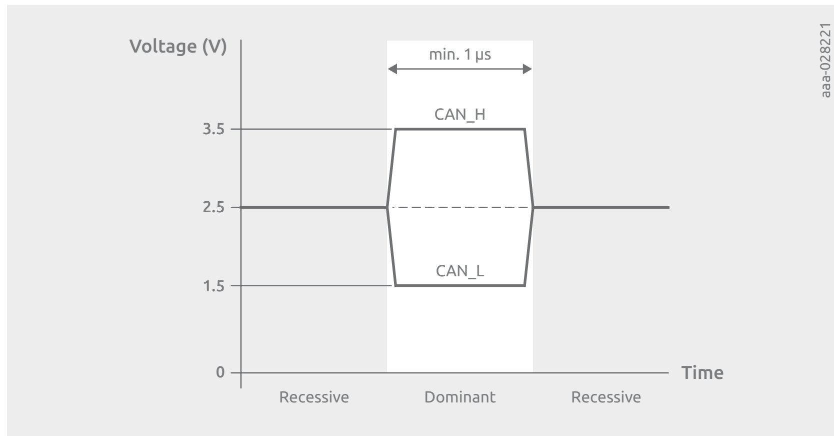


Figure 55 | High speed CAN Bus logical states

6.2.3 CAN FD

Because more and more ECUs are used in an automotive network with the requirement to transmit and receive more data, the classical CAN network with its limitation to 1 Mbit/s is considered insufficient for future needs. CAN FD is an update of the physical layer of CAN [23]. A major difference is a flexible data rate, that is defined up to 5 Mbit/s. 2 Mbit/s is the typical implementation limit suitable for many applications that do not require higher data rates. CAN FD uses the same differential signal levels as high-speed CAN. The increased data rate is achieved by shortening the dominant and recessive states in parts of a send message. This technique increases the requirements on the physical layer and, thus, might require ESD protection with lower parasitic capacitance. Typical values for a maximum capacitance are 6 pF or 10 pF, as defined by the system owner, usually the car OEMs.

6.2.4 CAN XL

For even higher data rates, up to 10 Mbit/s CAN XL is currently in the process of becoming a standard. Here, different techniques of actively increasing the signal quality and data rates are employed. CAN XL is designed to be compatible with 10BASE-T1s for easy integrability in a zonal architecture, see Chapter 7. It can be seen as an upgrade to CAN FD and probably will therefore require external ESD protection devices with lower capacitance than high-speed CAN.

6.2.5 Compliance testing for CAN, CAN FD and CAN XL

External ESD protection devices can be applied to the CAN_H and CAN_L line to extend the ESD robustness of the network, protect the CAN transceivers and ensure safe — not secure — communication. The industry offers devices specifically designed to protect two CAN bus lines from damage caused by ESD and other transients. The requirements on such an external protection device are set explicitly or implicitly, via system requirements, by the car OEM. Furthermore, there is the EMC compliance specification IEC 62228-3 [24] which, likewise to LIN, is testing an external ESD protection device in combination with a transceiver, thus also referred to as *combination test*.

The compliance test according to IEC 62228-3 describes a similar test to the compliance testing procedures used for LIN [16] and limits are set by the respective system owner or car OEM. Again, there is a dummy network consisting of three transceivers, but in contrast to LIN every transceiver is protected by an external ESD protection device, and four tests: emission of RF disturbances, immunity against RF disturbances, Immunity against transients and ESD. In detail the tests are conducted differently than the corresponding LIN tests.

In the emission of RF disturbances test, the dummy network is communicating while CAN_L and CAN_H are coupled capacitively to a common point. The test evaluates the conducted emission from this point. Two dummy communication signals are used: Signal 1, a 250 kHz signal with 50% duty cycle, and Signal 2, with 50 kHz and 90% duty cycle. Figure 56 shows a typical result of this measurement. Signal 1 leads to higher emission at higher frequencies, while Signal 2 leads to emission at lower frequencies — this is also due to the unbalanced lines from the 90% duty cycle. As with LIN, this test is usually not severely affected by a suitable ESD protection device.

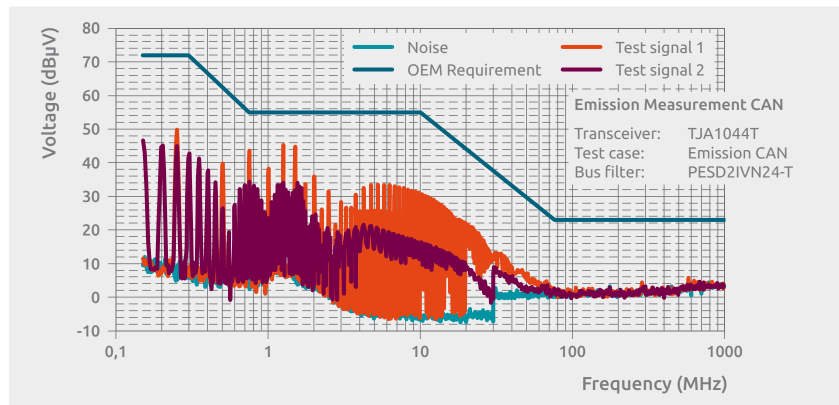


Figure 56 | Typical result of emission of RF disturbance test

The test for immunity against RF disturbances is a DPI test similar to the one used for LIN and using a capacitive coupling network to couple into CAN_H and CAN_L. Again, there is a test in active sleep mode. Furthermore, the coupling is done equally to CAN_H and CAN_L as well as unbalanced with +10% and −10%. The unbalanced cases are worst case tests and the OEM requirement does not necessary apply. Figure 57 shows typical results. The performance of the device in the test mainly depends on the breakdown or trigger voltage. The higher the voltage, the higher the power that is required to activate the result. On the other hand, a low clamping voltage is key for ESD protection performance. Therefore, a low dynamic resistance is the key parameter for a good ESD protection device that only has a minor effect on system immunity.

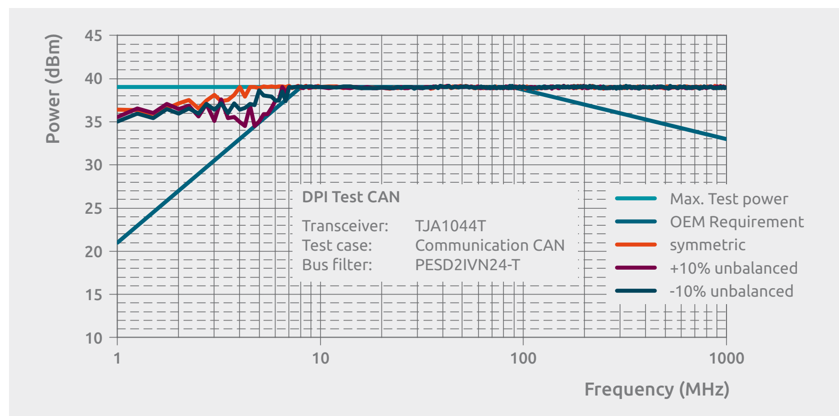


Figure 57 | Typical result of immunity against RF disturbance in active mode. The unbalanced cases are worst case tests and the OEM requirement does not necessary apply.

Similar to the test procedure for LIN, the immunity against transients test is based on the dummy network. It uses capacitive coupling, and applies Pulses 1, 2a, 3a, and 3b from ISO7637-2 [9]. The system is tested in active and sleep mode. In active mode, communications need to continue; while in sleep mode, the transceivers should not experience an unexpected wake-up.

The last test in IEC 62228-3 is the ESD test, which, unlike to the procedure for LIN, is only applied to the connector directly. Again, the reference module consists of a single transceiver, an external ESD protection and an optional CMC. Pulses according to IEC 61000-4-2 are applied to both connector pins of CAN_H and CAN_L. The functionality is tested using a curve tracer and with dummy communication. Modern ESD protection devices provide 30 kV system level robustness in this test.

Three parameters that are not captured in the IEC 62228-3 are usually directly set by the system owner or via other norms applicable: V_{RWM} (or breakdown or trigger voltage), the maximally allowed capacitance, and matching of the capacitances of both lines.

As CAN networks may be shorted to voltage sources, e.g. the car battery, ESD protection devices at the CAN_L and CAN_H lines must be able to withstand the higher voltage levels. In jump-start condition a minimum of 24 V is required as stand-off voltage V_{RWM}. There is no industry norm for checking this requirement. However, Ford Motor Company and Jaguar Landrover provide the CI270 specification [25,26] where an external ESD protection device has to withstand 28 V for 1 second.

The maximum capacitance that can be tolerated in the system depends on the topology, number of nodes, and cable length. Usually, car OEMs have requirements for the maximum tolerable capacitance of the external protection device, or the complete node. These requirements might change from platform to platform. Common values for maximum capacitance for CAN and CAN FD are 17 to 30 pF and 6 to 10 pF respectively. However, these values can significantly differ from OEM to OEM. Some OEMs do not differentiate in their requirements between CAN and CAN FD. Currently, CAN XL is too early in the phase of development and standardization to make a claim. However, assuming the same values as for CAN FD is realistic.

As CAN is a differential signal, the matching of the parasitic capacitance on both lines has an impact on signal integrity. Again, the relevance of this value depends on various features and OEMs have different views and requirements. A common maximum value is 2 to 10%.

6.3 FlexRay interface

Developed in 1999 by the FlexRay Consortium [27,28], the first FlexRay systems were introduced in 2006. It is a fault-tolerant, high-speed bus system, targeted at growing networking demands in Automotive, and suited for applications like X-by-Wire.

FlexRay can operate up to 10 Mbit/s per channel, using the differential signals BP and BM. In addition to single-channel operation (like LIN and CAN), it can be operated as a dual-channel system, making data available in a redundant network. The higher fault tolerance and higher transmission rates of FlexRay systems lead to higher system costs compared to CAN and LIN protocol-based networks.

For ESD protection diodes, the Application Note on the Physical Layer [29] proposes a low diode capacitance of < 20 pF, with a matching of less than 2%.

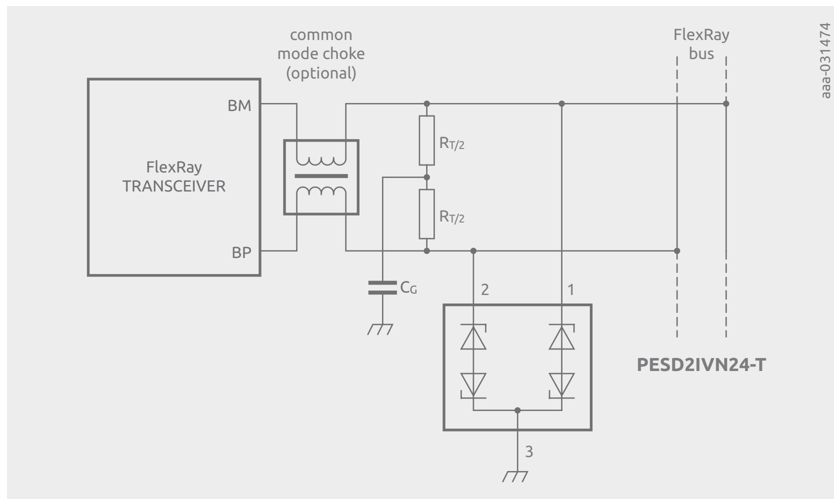


Figure 58 | Generic FlexRay interface

Figure 58 shows a FlexRay transceiver that is coupled via a common mode choke, a differential termination with twice $R_{T/2}$ and a bidirectional ESD protection to the bus.

Chapter 7
Zonal architecture

Three major trends currently dominate developments in the automotive industry: electrification autonomous driving, and connectivity. While the first has a massive impact on the power train and high-voltage part of the wiring harness, the last two are driving a paradigm change in the way electric control units communicate in the car. Trends and concepts known from consumer electronics, communication infrastructure, and IoT are being transferred to the vehicle and go alongside with trend of ever-increasing data rates. From the perspective of the in-vehicle network autonomous driving and connectivity translate to higher data rates and a zonal architecture.

The way a current in-vehicle network topology looks like can only be understood considering the historic background. The first electric control interfaces in a vehicle connected the controller and actuator via a single wire. As the demand for functionality increased, bus networks were introduced. Here, the buses connected control units of a functional unit of a car, like the power train or body control. This scheme can still be identified in today's cars, even though it has expanded due to the increased demands of bandwidth and interconnection. The idea to implement physically separated buses to fulfill security requirements makes the topology even more complex.

If one starts designing an in-vehicle network from scratch, it will probably look different. Modern mechanisms like decoupling of physical addresses and software addresses, plug-and-play configurability and end-to-end encryption (like the VPN we are using to work from home) would be expected as readily available. Today's in-vehicle networks do not provide these features and retrofitting is expensive and does not work properly in many cases. In contrast to the historic way of connecting the ECUs that need to talk to each other directly, zonal architecture aims to form a network where in principle any ECU can talk to any other. To do so every ECU is connected to a domain or zone controller directly via a short CAN, LIN, or 10BASE-T1s interface. The domain or zone controllers are connected using a high speed (often 1000BASE-T1 is proposed) backbone network.

Using software, the system gets extremely versatile: Virtual CAN/LIN networks can be implemented, so that legacy ECUs can operate as if there was an old-fashioned CAN/LIN only topology. As every ECU gets a dynamic IP, plug-and-play as well as reconfigurability (e.g. with an update over the air) are possible. On software basis secure sub-networks can be formed to ensure compliance in safety critical applications and protect sensitive data.

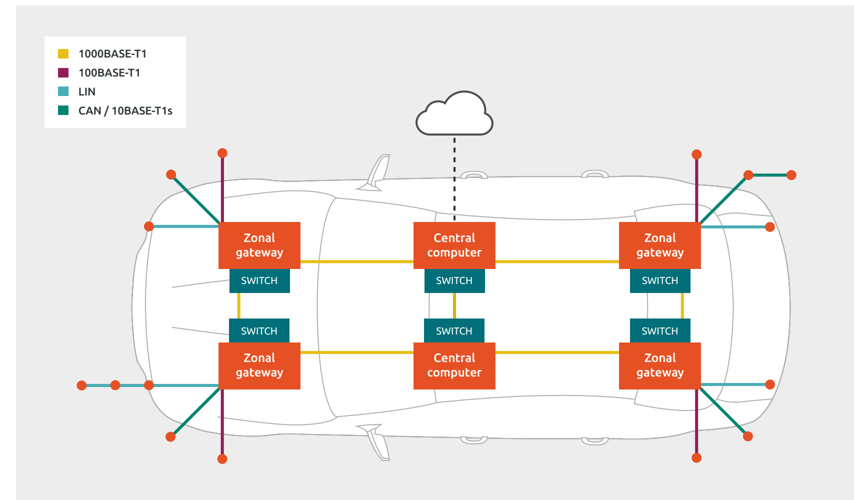


Figure 59 | Zonal architecture of the in-vehicle network

Automotive Ethernet is the system of choice for such a topology, as it inherently provides the desired features of flexibility. Furthermore, it is easy to use by engineers as it is the standard technology in today's communication infrastructure. The different speed classes are designed to suite the three different stages of the zonal architecture: 1000BASE-T1 and multi-gigabit for the connection of the zone controllers, 100BASE-T1 for the direct connection of ECUs to the zone controller; and 10BASE-T1s to connect several ECUs with a limited demand for bandwidth to a zone controller.

This enables an "all IP car" solely using automotive Ethernet. The expert community is split if this will come in future or if it is even desired. The general consensus is that legacy protocols like LIN, CAN (FD/XL), and FlexRay will stay in the zonal architecture for the next decades for cost and legacy reasons. The exception to the zonal architecture that experts can agree on, can be found in the high-speed connection of ADAS Sensors to their respective control units. Here, no flexibility is required, and a mostly uni-directional high-bandwidth data stream needs to be transmitted. The technology of choice, SerDes interfaces, fulfil exactly this purpose.

7.1 Automotive Ethernet

Automotive Ethernet emerged in the beginning of the 2010s under the name of BroadR-Reach with a speed of 100Mbit/s. To establish a standard, the OPEN Alliance SIG [30] was formed. They have standards and test procedures for *100BASE-T1*—the successor of BroadR-Reach—and *1000BASE-T1*, the 10 times faster version. Currently, *10BASE-T1s* and multi-gigabit (2.5 Gbit/s, 5 Gbit/s, and 10 Gbit/s) Ethernet is in preparation. The postfix -T1 indicates a single twisted-pair cable is used. Generally, unshielded twisted-pair (UTP) and shielded twisted-pair (STP) are allowed. However, for costs reasons, UTP is preferred. At data rates of 100 Mbit/s and above, all connections are point-to-point and a central switch is required to create larger networks. The low-cost 10BASE-T1S however, allows several nodes to be connected to a single UTP cable. The physical layer is very close and sometimes compatible with CAN (FD/XL). The work in the OPEN Alliance is coordinated with other groups like NAV Alliance and serves as preparation and augmentation for standards published via IEEE, SAE, and other standardization consortiums.

As with every automotive networking technology, the ESD requirements for automotive Ethernet are rather high. Usually, 15 kV contact discharge (IEC61000-4-2) on a module basis is the standard requirement, but some car OEMs may ask for 30 kV air discharge. In most test procedures demanded by car manufacturers, ESD is tested on the unpowered module with direct discharge on the communication pins and on the powered module with a connected cable. After the unpowered test, the module is connected to a reference system and checked for normal operation. Effects that may cause a failure in the unpowered test are destruction or a damage of the PHY and degradation of passive components in the signal path deteriorating signal integrity. In the powered test, there is the possibility of a non-destructive event in the PHY causing malfunction and errors in communication. This failure is usually called soft-failure. A suitable ESD protection concept for an automotive Ethernet interface should prevent the PHY and passive components from destruction, degradation, or malfunctioning from an ESD event, without impacting the system performance in any negative way.

In the *system implementation specification* for 100BASE-T1 [31], the OPEN Alliance proposes two possible external ESD protection devices. As shown in Figure 60, one can be placed at the connector (ESD_1) and one at the PHY (ESD_2). The specification allows to use none, one, or both devices to achieve the desired ESD robustness. The external ESD protection at the PHY is considered a part of the PHY from the view on the specification. Hence, the PHY in combination with the external protection needs to pass all requirements that apply to the PHY alone. The protection at the connector must comply with the OPEN Alliance specification for external ESD protection devices [32]. From a system perspective, the external ESD protection at the connector is superior and the best way to design a robust interface. Before comparing both protections and the impact on the systems ESD robustness, we take a closer look at the specification for external ESD protection devices and how ESD events propagate in the interface.

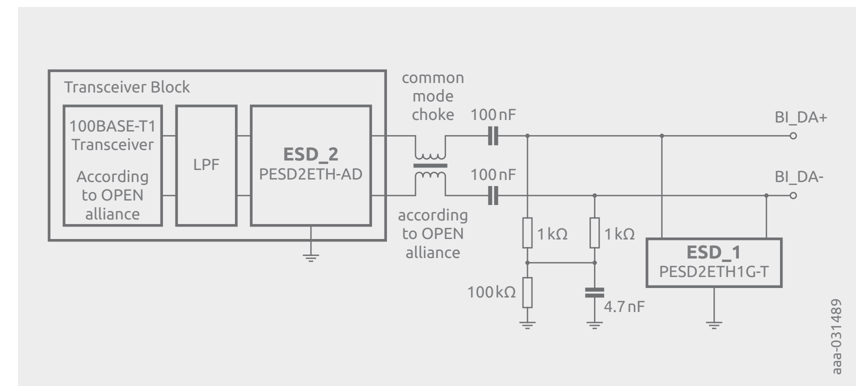


Figure 60 | Interface topology for 100BASE-T1 according to OPEN Alliance [31] with placement of ESD protection at the connector and as part of the transceiver block

7.2 Dynamic of an ESD event in an 100BASE-T1 interface

Before comparing both possible options for ESD protection, lets have a look at how ESD propagates through the MDI (Media Dependent Interface — in OPEN Alliance this refers to the generic interface structure). As depicted in Figure 60, the interface consists of the common-mode termination (CMT), decoupling capacitors, the CMC, and the transceiver block. The transceiver can be a PHY, which would be the IC that is used in an ECU or a switch which is the IC on the opposite module, usually a gateway.

Considering an unprotected MDI, an ESD event injected at the connector first sees the CMT in parallel to rest of the interface. The current divides: some current is flowing to ground through the CMT while the rest is flowing through the decoupling capacitors or is reflected. The energy flowing through the CMC heats up the resistors and thus degrades them. ESD is an event with a bandwidth up to the single digit GHz range. Therefore, the decoupling capacitors are practically invisible.

The most complex behavior with the ESD pulse is observed at the CMC. The behavior can be split into three different effects. The ideal behavior of the CMC, the series inductance, and the saturation that is caused by the ferrite core. In the MDI, the CMC is used to suppress common mode noise, where the current is flowing in the same direction on both signal lines, and to pass through differential mode signals, where the currents are flowing opposite directions. In case of an ESD event, there is a current on one signal line only (when neglecting crosstalk and coupling before the CMC). Technically, this is a superposition of a differential and common I_{ESD} on line 1:

$$\begin{pmatrix} I_{line1} \\ I_{line2} \end{pmatrix} = \begin{pmatrix} I_{ESD} \\ 0 \end{pmatrix} = \underbrace{\begin{pmatrix} +{}^{1}/_{2}\, I_{ESD} \\ +{}^{1}/_{2}\, I_{ESD} \end{pmatrix}}_{Common\ mode} + \underbrace{\begin{pmatrix} +{}^{1}/_{2}\, I_{ESD} \\ -{}^{1}/_{2}\, I_{ESD} \end{pmatrix}}_{Differential\ mode}$$

As the common mode is suppressed, the CMC enforces a current in the opposite direction on the signal line that is not hit by ESD. At the PHY, this has two implications. The current flowing into the pin on the signal line where ESD was injected is reduced and at the other pin a negative voltage is seen. Depending on the internal structure, the current flows in a loop, into the pin in the line where ESD injected and out on the other line and ground. The PHY or the external ESD protection in front of the PHY needs to handle this event. When placing the external ESD protection directly at the connector, this event is significantly reduced.

The second effect of the CMC being a series inductance is beneficial from a system robustness perspective. The fast-rising edge of an ESD pulse is affected by the inductance as well as the resistive parameters. In the first picosecond, the pulse basically sees the parallel connection of the parasitic inductance of the CMT and the series inductance of the CMC and the PHY. Hence, the first fast-rising peek of the ESD event is going to be suppressed. This makes the interface in general more robust. However, the "slower" part of the event is still flowing through the CMC, will heat it up and potentially lead to a deterioration of symmetry. This current is in practice larger than one might assume due to the effect of saturation.

Figure 61 shows TLP measurements on a single channel — and the other channel left open — of a CMC compliant with 100BASE-T1. An equivalent circuit representation of the measurement setup is shown in Figure 62. There are three different modes of operation that can be distinguished: (I) first, the coil acts a single inductor while the magnetic field builds up; (II) the CMC operates as a transformer and transforms the open of the unused channel to the channel that is measured, nearly no current is flowing; and (III) after a certain time, the accumulated magnetic field in the core goes into saturation and the behavior becomes ohmic. Here, the equivalent resistance is 2 Ω. This value varies from device to device, but the value is usually in this order of magnitude. In a real-life implementation, the channel that is open in this measurement would be connected to the PHY on the one side and the CMT of the other side. This in fact changes the TLP measurement results, even though the general behavior remains the same.

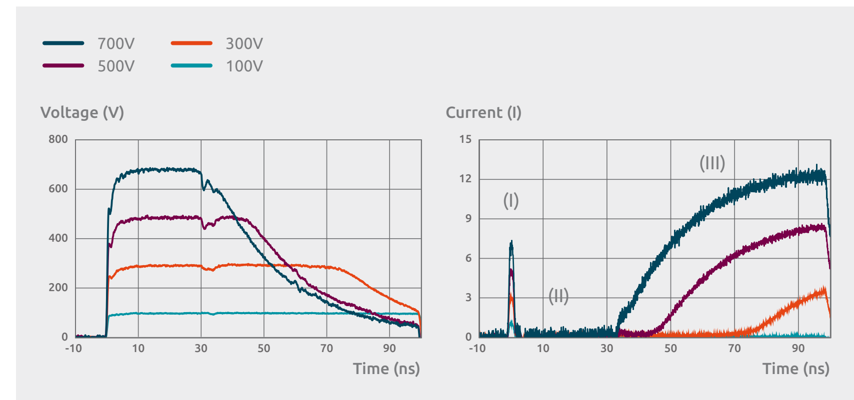


Figure 61 | TLP measurement of a single channel of a CMC for 100BASE-T1

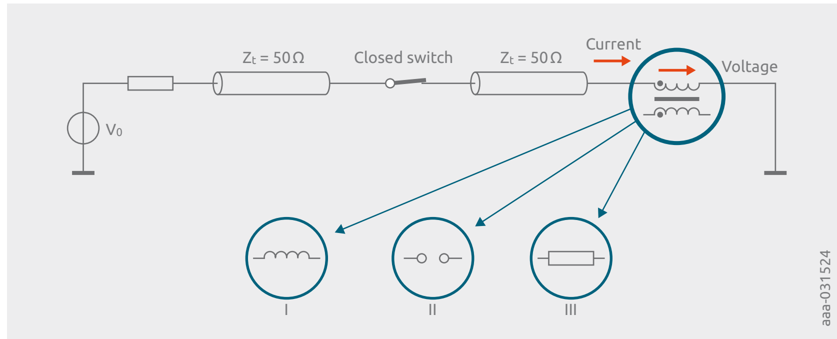


Figure 62 | Equivalent circuit representation of the behavior of a CMC in TLP characterization

From this measurement, the CMC is beneficial in the ESD event, but only until saturation is reached. Then, the CMC becomes an ohmic resistor of about 2 Ω and offers no protection. Furthermore, in this ohmic case, a high current is flowing through the CMC potentially harming it. This becomes evident when looking at the power plotted in Figure 63. Hence, an external ESD protection that is in front of the CMC—at the connector—should prevent the CMC from going into saturation to achieve the performance for the system.

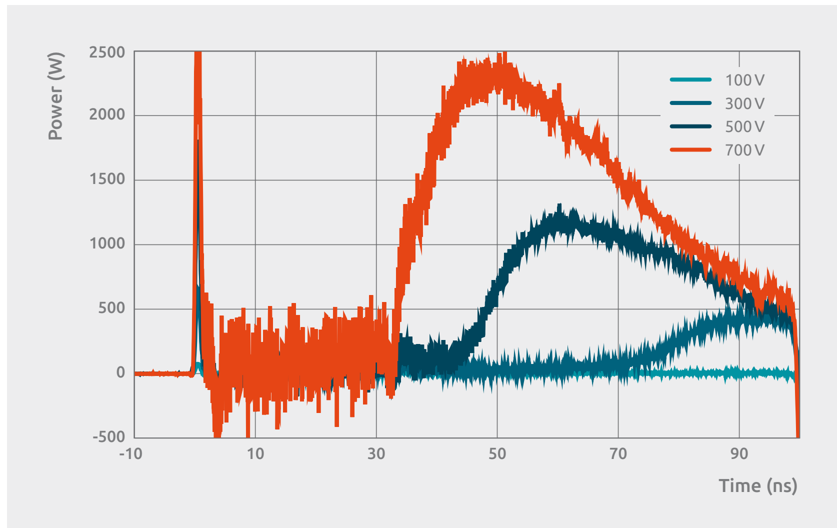


Figure 63 | Power loss at the CMC during the TLP tests shown in Figure 60

7.3 Comparison of protection schemes

Previously, we discussed how an ESD behaves in the MDI and interacts with the different components. From a theoretical standpoint, it is clear that a protection at the connector (ESD_1) is favorable to achieve a high system level robustness. This not only protects the PHY, but also prevents the passive components from degrading because of the extraordinary stress during an ESD event. These considerations are also supported by practical measurements as shown here.

Three different configurations are analyzed using an EMI Scanner[1]. An generic MDI without external ESD protection ❶, with an external ESD protection device at the PHY ❷, and with an external ESD protection at the connector ❸. In the measurement setup, a TLP like pulse of 500 V amplitude is injected into BI_DA+, a H-field probe is located closely above the PCB, recording the magnetic field during the event. A robotic arm moves the H-field probe to the next location and the next pulse is injected. This way the magnetic field in x- and y-dimension is recorded at thousands of locations on the PCB. The magnetic field is linearly related to the current flowing on the surface of the PCB. This way, the vectorial current flow during an ESD event can be visualized.

Figure 64 shows the amplitude of the current for the three cases at the same point in time. The color scale reflects the current amplitude from blue (0 A) to red (maximum current). The external ESD protection at the PHY does not reduce the energy flowing through the CMT and CMC and only has rather small impact on the current flowing into PHY. The ESD protection at the connector, however, effectively protects the CMT, CMC, and PHY.

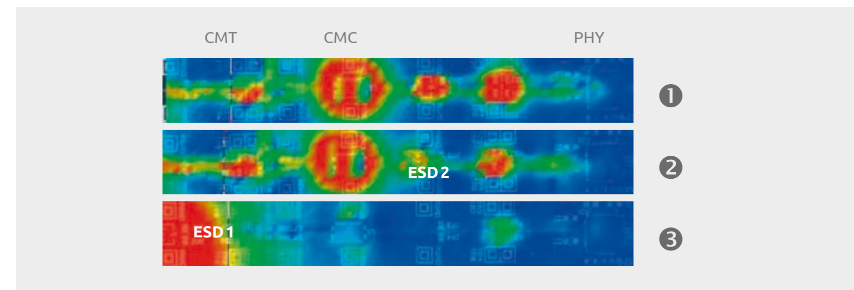


Figure 64 | Current amplitude during and ESD event for the MDI without ❶ and with external protection at the connector ❷ and at the PHY ❸. The color scale reflects the current amplitude from blue (0 A) to red (maximum current).

1 Amber Precision Instruments, SmartScan 350

Furthermore, the measurement setup can be used to visualize the complex behavior of the CMC. Figures 65 and 66 respectively show the current flow at the CMC without external ESD protection and with external ESD protection at the connector at the same points in time. In the first picture, the pulse arrives at the CMC. The difference in both setups is mainly in the amplitude of the current on the traces before and after the CMC. After 15 ns, the CMC operates mainly as a transformer and is enforcing the differential mode on the traces. This can be seen by the arrows pointing perpendicular to the parallel traces. In the case without the external ESD protection, this effect is significantly stronger than in the case with the ESD protection at the connector. This illustrates that there is no effect of a negative voltage swing on the data line that is not affected by ESD or at least it is significantly reduced when using an external ESD protection at the connector.

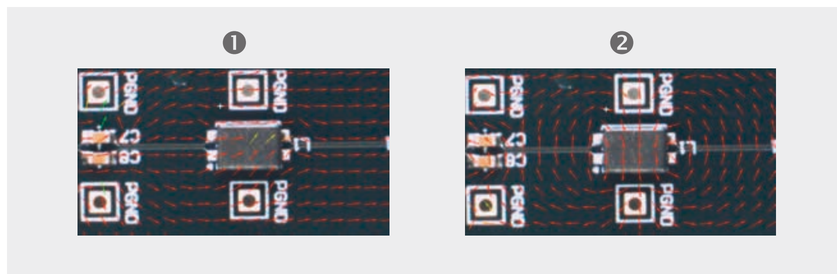


Figure 65 | Current vector at CMC without ESD protection at 1 ns ❶ and 15 ns ❷. ESD is injected at the lower trace from the left side.

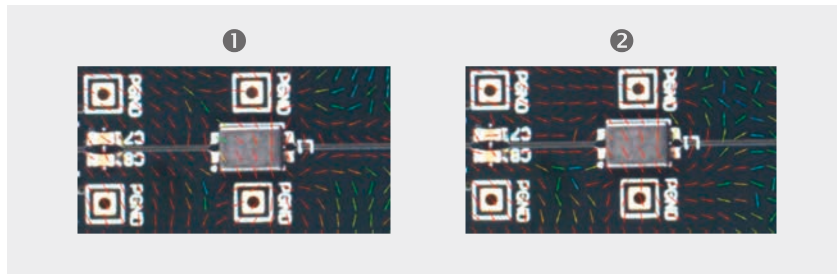


Figure 66 | Current vector at CMC with ESD protection at the connector at 1 ns ❶ and 15 ns ❷. ESD is injected at the lower trace from the left side.

7.4 OPEN Alliance compliance measurements for 100BASE-T

To be suitable for the use at the connector, the OPEN Alliance states several requirements on the external ESD protection device. The document [32] applicable for 100BASE-T1 demands five technical parameters: bi-directionality, DC operating voltage of more than 24 V, a trigger voltage of above 100 V, ESD robustness of the device according to [6] level 4, and the minimum requirement for 1000 discharges. The 24 V operation capability is required to withstand short-to-battery scenarios, while the 100 V trigger and bi-directionality shall improve the performance during RF immunity testing. The ESD robustness with the increased number of discharges is needed to limit the risk of degrading parameters over time. Additionally, four different tests are required for compliance: S-Parameter measurements, ESD robustness, discharge current, and unwanted clamping.

The "Mixed Mode S-Parameter Measurement" test evaluates transmission, reflection, and the conversion from differential to common mode. The transmission and reflection compliance requirement substitute the requirement for a maximum parasitic capacitance. The limits stated in [32] correspond to a capacitance of about 5 pF. The mode conversion is measured to assure the matching of the parasitics of both channels are in compliance. Even though the measurement is going to very low amplitudes and requires profound measurement skills, the deviation in terms of the capacitance allows more than ten percent if the absolute capacitance is about 3 pF. Figure 67 shows typical results of S-parameters for the PESD2ETH1G-T with 1.8 pF.

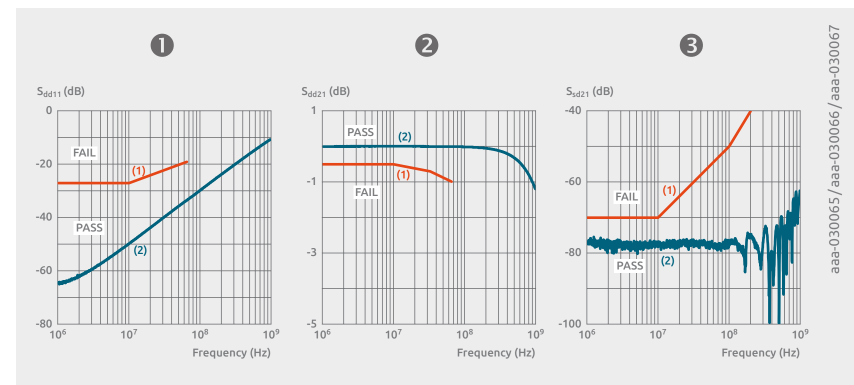


Figure 67 | Transmission ❶, reflection ❷, and mode conversion ❸ of PESD2ETH1G-T with 1.8 pF and a matching of 0.5% typical. Limits according to OPEN Alliance 100BASE-T1 [32].

The "Damage from ESD" measurement is more advanced than usual robustness test. Primarily checking if the device is operating normally, it also accounts for degradation. First S-Parameters are measured, similar to the previous test, but on a modified PCB. Next ESD is applied to all pins of the external ESD protection device, and the parameters are checked again. In [32], an IEC61000-4-2 pulse with +/− 8 kV is applied 20 times per polarity to all pins. The S-parameters cannot deviate more than 0.1 dB for transmission and 1 dB for reflection and mode conversion for frequencies below 200 MHz. Silicon-based ESD protection devices are usually not affected in this test, while varistor technology is in principle more sensitive. Figure 68 shows typical results. Please note that other PCBs are used than in Figure 67 resulting in different graphs.

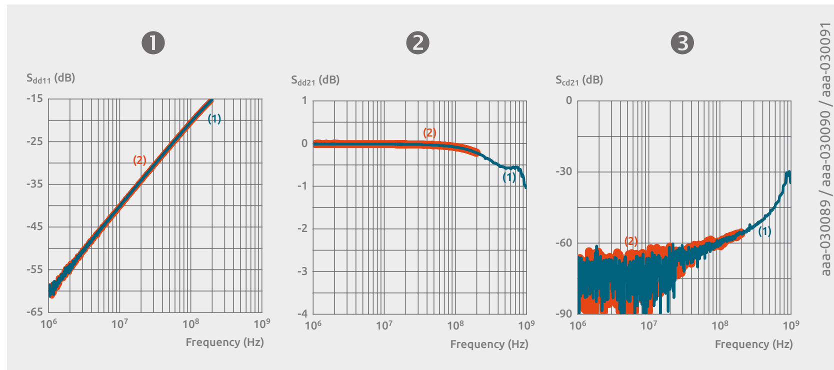


Figure 68 | Transmission ❶, reflection ❷, and mode conversion ❸ of PESD2ETH1G-T before ESD (1) and after 20 repetitive discharges of ±8kV at every pin (2)

The third test is called "ESD Discharge current measurement" and aims to predict how good an external protection device can protect the PHY. To do so, a dummy MDI is setup, where the PHY is replaced by a resistor network of 2 Ω, modelling the behavior of the internal ESD protection in the PHY. The current flowing though resistor network is recorded while shooting an IEC61000-4-2 pulse at the input. To comply, the current should not exceed certain limits. There are several classes referring to different HBM ratings of PHYs. The specific values published in [32] are obsolete, as it states a 50 Ω resistor to replace the PHY and outdated limit lines. Furthermore, the test setup is modified to be conducted with two different CMCs, as the saturation characteristic have a significant impact on the outcome of this test. The intention of the test is to have a general result, such as: "If you use this external ESD protection device at the connector, a PHY with 2 kV HBM rating will be protected against an 15 kV IEC61000-4-2 discharge at the connector". Please note that this has a unidirectional implication. Passing the test gives high confidence that the PHY will be well protected, while failing does not give any specific indication.

Figure 69 shows results for +8 kV, +15 kV, and +25 kV for the PESD2ETH1G-T. Even though results show a fail for +25 kV and a 2 kV HBM PHY, experiments show in practice 2 kV HBM PHYs are well protected at 25 kV.

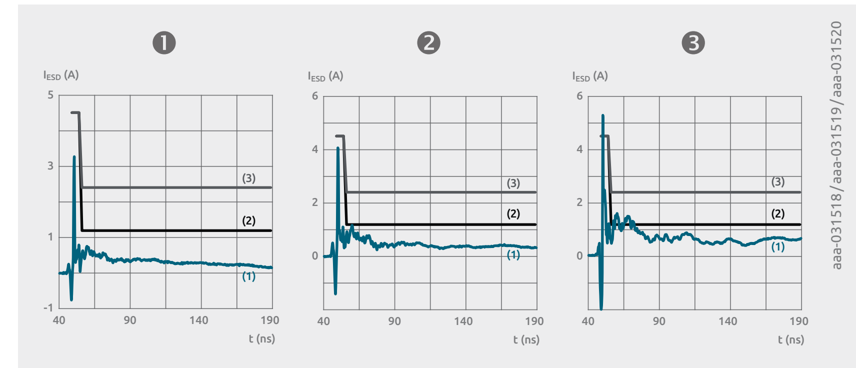


Figure 69 | Results of ESD Discharge current measurement for +8 kV ❶, +15 kV ❷, and +25 kV ❸ for the PESD2ETH1G-T (1) with the limit line for 2 kV (2) and 4 kV (3) HBM PHYs

Technological differences of ESD protection devices can have a significant impact on the result of this measurement and thus on the resulting ESD robustness of the interface. The interplay of the saturation characteristic of the CMC and the clamping behavior of the external ESD protection are the most important factors. Clamping needs to be as low as possible, to prevent the CMC from going into saturation. However, the requirements of a trigger voltage and the "unwanted clamping" test, described in the next paragraph, need to met as well. There are currently three major technologies that might be applicable as ESD protections: Zener diodes, advances silicon technologies (such as SCRs, open-base transistors and other snap-back technologies), and varistors. From the RF requirements of the interface it is clear that a Zener diode is not an option, only silicon based or varistor technology can be used. Silicon technology can make use of the snap-back effect resulting in very low clamping voltages while meeting the other requirements of norm. Varistors are also available with suitable RF behavior and high trigger voltages. However, the clamping voltage is significantly higher. This can be seen in the TLP graph comparison in Figure 70 together with the resulting discharge currents at 6 kV. The snap-back and thus resulting very low clamping of the PESD2ETH1G-T provides superior protection to the varistor based solution.

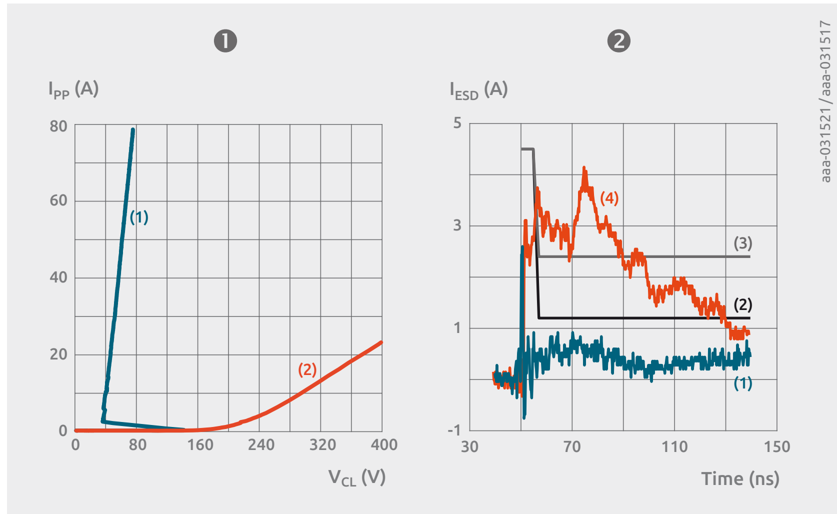


Figure 70 | TLP Graph ❶ of silicon based protection PESD2ETH1G-T (1) and a varistor (2) and the corresponding ESD discharge current measurements ❷

To simulate a similar test to the DPI that is used for CAN, the "Test of unwanted Clamping Effect at RF immunity Tests" is required. Here the external ESD protection is connected to a CMC and both are exposed to common-mode signals of high amplitude, while the common mode rejection is measured. As the power of the common-mode signals is increased, the common-mode rejection is not allowed to change. Additionally there can be no changes in the common-mode rejection related to ESD protection that is high-ohmic and has triggered. Meaning the presence of external ESD protection can only have a negligible impact on the results of RF-immunity tests of the MDI up the maximum tested power. Figure 71 shows the result for the PESD2ETH1G-T. The curves lying on top of each other is an indication that the device is not triggering.

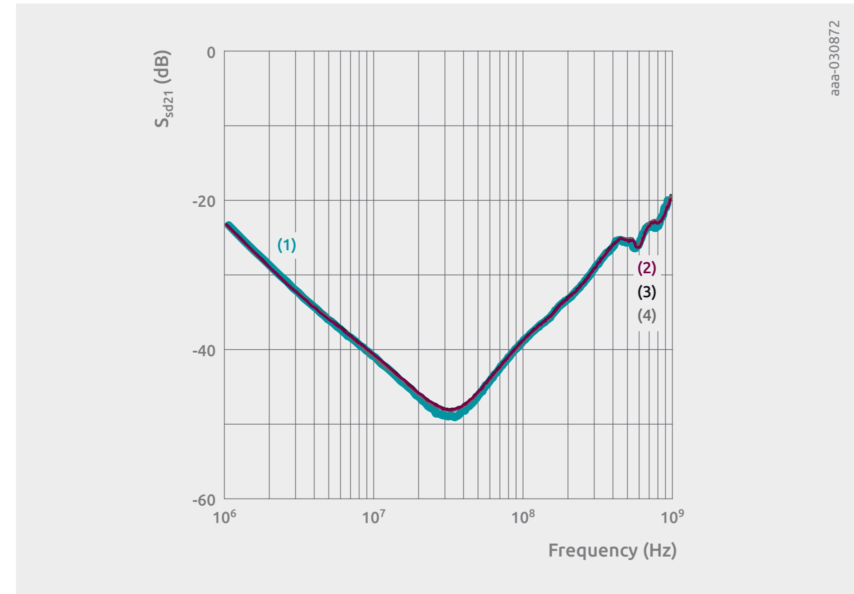


Figure 71 | Test of unwanted Clamping Effect at RF immunity Tests of PESD2ETH1G-T with reference at 25 dBm (1) and increased power levels of 33 dBm (2), 36 dBm (3), and 39 dBm (4). The device is not triggering.

7.5 Current state of compliance tests for 1000BASE-T1 and 10BASE-T1s ESD protection

At the point this handbook is published, the only publicly available document on these tests is [32]. However, this document is already outdated and successor versions are being discussed in technical committees for 100BASE-T1, as well as 1000BASE-T1, 10BASE-T1s, and multi-gigabit ethernet. The current state of discussion has been addressed above. For 1000BASE-T1, basically the same test procedure with adaptions of the S-parameter limits and the usage of 1000BASE-T1 compliant CMC is planned. For 10BASE-T1s and multi-gigabit Ethernet, the discussion on the physical layer are still at an early stage.

Chapter 8

SerDes – Serializer / Deserializer interfaces

Serializer/deserializer (SerDes) is an umbrella term for interfaces using serial interface to transmit data that is available from a parallel data stream. These interfaces are high bandwidth, point-to-point by design, and latency is usually not critical. The interfaces mainly operate unidirectional or bidirectional where the bandwidth in one direction is significantly higher than in the other. The physical implementation of the serial data stream can be differential using low voltage differential signaling (LVDS) or single ended using a coaxial cable. Optical links are also possible but they will not be discussed here. Furthermore, SerDes interfaces with a single ended physical layer are sometimes used to transmit power to the ECU additionally to the data stream. For coaxial single ended links, this technique is called Power-over-Coax (PoC) in similarity to Power-over-Data-line (PoDl) or Power-over-Ethernet (PoE).

SerDes interfaces are mainly used to transmit video data. The most common applications are in infotainment to connect displays, body and convenience applications like parking cameras, and cameras used for ADAS applications. Especially for cameras, the PoC functionality is very attractive. In the modern zonal architecture, SerDes interfaces are the exceptional point-to-point connections that are required to make high-resolution sensor data available.

For SerDes, proprietary solutions are common in the automotive domain. Currently there is an initiative ongoing to standardize SerDes interfaces for automotive applications [33]. However, at the time no standard is available. Here, we will shortly address three different proprietary implementations to provide a brief overview.

The requirements for external protection are similar for all SerDes interfaces and state-of-the art protection technology is required. Protection devices used in the computing segment to protect high-speed data lines with extremely low capacitance are suitable for this task. Often multiline protection devices that are designed for USB are used to protection LVDS interfaces. A low parasitic capacitance is essential to maintain signal integrity. As the parasitic capacitance is lower than 1 pF, the matching of line capacitances is not critical and single line protection devices are applicable. Single ended coaxial interfaces are protected using single line protection devices.

8.1 APIX – Automotive Pixel Link

Automotive Pixel Link (APIX) was designed by Inova Semiconductors and licensed in 2008 by Fujitsu. It can be used to transmit digital video signals over a distance up to 15 m. Third generation APIX3 has been available since 2016. From APIX2 the standard supports bi-directional protocols in addition to one-direction video transmission. APIX2 support a 720 p video signal and additional communication over SPI, I²C, or Ethernet over the same interface. APIX3 supports data rates up to 6 Gbit/s. Depending on the operation mode, one or two STP or shielded quad-wire twisted pair are required. Furthermore, it allows data lines to be used as power supply for the modules. With *Power-over-APIX* (PoA), the differential data lines can also be used to provide power to the serializer side.

When PoA is used, the protection must be selected accordingly. Either, the protection is located behind the decoupling capacitor so the same protection that would be used without PoA is used. Or, the protection is located at the connector. In that case, the protection is not allowed to clamp below the supplied DC voltage to prevent latch-up. The comments for PoC in Section 8.5 also apply to PoA.

8.2 FPD-Link – Flat Panel Display Link

Flat Panel Display Link (FPD-link) was originally designed for displays but is also very common to connect cameras to ADAS computing units. It was designed in 1996 by National Semiconductors for the use in laptops and TVs. Today, FPD-link is owned by TI and very popular for automotive ADAS applications. The second generation FPD-link introduced communication via a single LVDS channel on a STP cable with up to 10 m, achieving up to 1.8 Gbit/s. FPD-link III allows for data rates up to 13.3 Gbit/s and bi-directional communication on a single link. Additionally, FPD-link III allows the usage of coaxial cables and PoC. FPD-link serializes a parallel TTL, LVCMOS, LVDS signals, or MIPI.

8.3 GMSL – Gigabit Multimedia Serial Link

Gigabit Multimedia Serial Link (GMSL) is a proprietary SerDes interface by Maxim Integrated mainly used for camera applications. The second generation was introduced in 2017 and features LVDS over STP and single ended coaxial operation with cables up to 15 m. The maximum data rate goes up to 3.1 Gbit/s and interfaces with LVCMOS, CMOS, LVDS, MIPI and HDMI. Communication is unidirectional with a bidirectional control channel. Furthermore, GMSL supports PoC with 5 and 12 V.

8.4 MIPI A-PHY

The MIPI Alliance comprises several standards for transmission video data, see Section 9.3 for details. With a comparable goal as the Automotive SerDes Alliance (ASA) [33], the MIPI Alliance is preparing a non-proprietary SerDes Standards called A-PHY [34]. The first version is announced to be released in 2020 and features up to 16 Gbps on cables up to 15 meters length. A-PHY shall support differential communication on STP cables and single-ended on coaxial cables also featuring power-over-coax. MIPI A-PHY is meant to directly interface with the existing MIPI Physical Layer Standards C-PHY and D-PHY and operate in the CSI-2 protocol.

8.5 Power-over-Coax (PoC)

Power-over-Coax (PoC) is very common and widely used especially with GMSL and FPD-link cameras in surround view and ADAS applications. The general principle is shown in Figure 72. Power is supplied to the serializer side from the deserializer side using appropriate filters, here simple inductors L1 and L2 and decoupling capacitors (decaps). The EMC requirements of the power source and regulator are very high to maintain signal integrity and not to spoil the data signal.

There are different possibilities to place external ESD protection devices. The goal is here to protect the high-speed interface. The power regulator input and power source output can be protected by ordinary TVS devices behind the filter. For the high-speed interface the protection can be placed at the connector (ESD_1), behind the decap (ESD_2), or both.

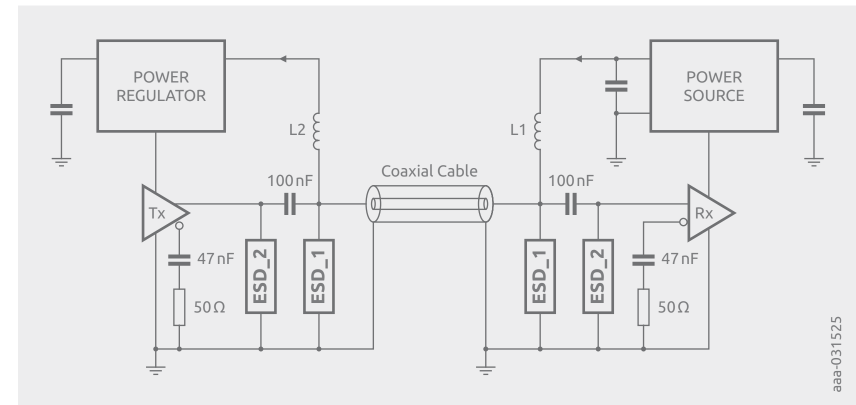


Figure 72 | Generic interface for SerDes with PoC and two positions for ESD protections

The placement at the connector should always be preferred, because it leads to the best protection performance. However, the protection device must be selected in a way that it can operate with the DC bias. For protections behind the decaps, only the data signal levels need to be considered. In general, snap-back devices are also applicable at the connector if there is no risk of latch-up. As it is very difficult to assess this situation on a purely theoretical level, in-application test are inevitable to ensure the application is protected and there is no risk of latch-up. The challenge is that in the application, a snap-back seen in TLP and a risk of latch-up do not necessarily correlate. There are devices that show a small snap-back in TLP but do not latch-up when tested in the lab. On the other hand, there are device that show a snap back in TLP but can latch-up at voltages lower than seen from TLP when stressed with surge pulses.

This different behavior depends on the technology and details in the implementation, and cannot be expressed in general terms in the datasheet as the results may vary with the applied DC source and the applied pulse. When testing for a latch-up, it is important to use the same power supply characteristics, in terms of load line and regulation scheme and speed. In many cases, the sources used in the application are not able to provide enough current within the short time of a transient event to actually cause a latch-up. Devices with a rather shallow snap back, are usually very robust against latch-up. On the other hand, some technologies show several snap backs which may not be seen from the datasheet because they are only triggered with very long pulse durations. A latch-up test with a realistic power supply and the relevant transients provides clarity and confidence.

The use of two external ESD protection devices at the location before and after the decap normally leads to increased ESD robustness. If the robustness achieved with one device is not sufficient, it is reasonable to consider populating the second location. However, the resulting behavior can become very complex and may cause effects that might not have been expected at first sight. Figure 73 shows the voltage at the IC with a protection device with snap back at the connector and an additional one behind the decap for an 8/20 µs surge pulse. The energy of the pulse is reduced by adding a second device. However, negative voltages are observed. The reason is that the device behind the decap triggers first reducing the voltage from 12 V to 5 V at the IC. At about 5 µs, the external ESD protection device at the connector is triggered as well and reduces the voltage by about 9 V. As the voltage at the IC is already at 5 V, the voltage becomes negative. For most ICs this is not a problem at all. However, the complexity of two non-linear devices needs to be kept in mind when designing such systems and trouble-shooting.

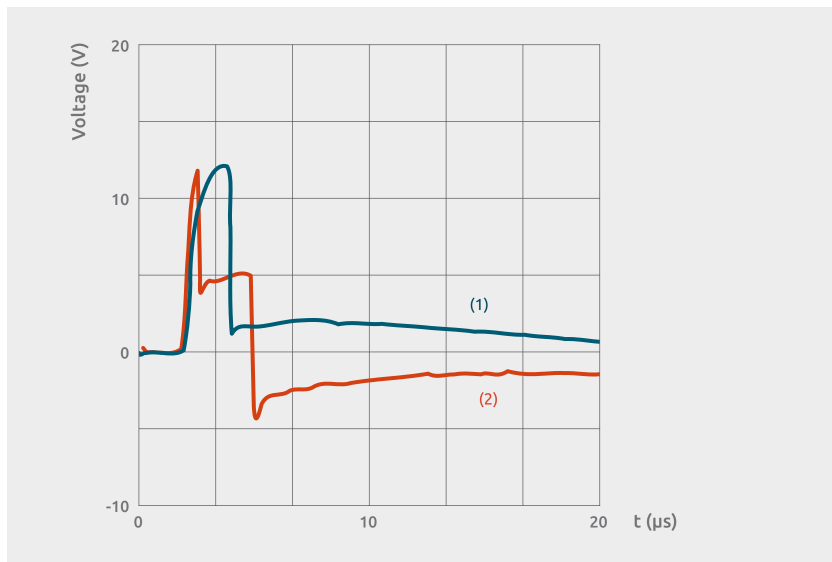


Figure 73 | Voltage at the IC according to Figure 72 with an 8/20 µs pulse of 15 V amplitude injected at the coaxial connector. ESD_1 is equipped with PESD9V0C1BSF. ESD_2 is not placed (1) and equipped with PESD3V3Z1BSF (2).

Chapter 9

Multimedia interfaces

Today's cars are more and more connected. When looking at advertisements, there was a clear shift of car OEMs from promoting the mechanical features of the car, like performance, to advertising connectivity, infotainment, and multimedia features next to safety. Consistently, the number of multimedia interfaces in cars are rapidly increasing. USB is already a standard interface in cars of all classes, high class cars feature USB 3 with power delivery capability that can charge a laptop. Many interfaces that are known from consumer electronics can be found throughout the car. However, they have to comply with much harder requirements in terms of reliability and robustness. Usually, these interfaces are not used in safety critical applications but customers expectations and the cost of replacement is much higher than the consumer electronics market.

In terms of ESD protection, the same devices as used for consumer products are applicable. Depending on the actual application, additional requirements like AEC-Q101 qualification and side-wettable flanks to allow automated optical inspection (AOI) for leadless packages are demanded. Requirements like short-to-battery robustness, as it is common for IVNs, are usually not considered for multimedia interfaces.

9.1 USB interfaces

USB interfaces are standard in infotainment systems of todays cars. They are used to connect mobile phones, USB sticks, and laptops with diagnostics software. USB 3 and high-speed charging using USB PD are getting more popular. Additionally to direct user interaction, USB is sometimes used to connect headrest displays and other periphery to the main infotainment system. Moreover, USB is discussed to be used in more critical applications like black-box, tachograph and debugging and interfaces of ADAS systems.

9.1.1 USB 1.0 and USB 2.0 interfaces

Table 11 shows an overview of contemporary USB standards and their related symbol rates.

Table 11: Overview of data rates for USB interfaces

USB Type	Speed class	Bit rate	Symbol rate (Baud rate) Coding method
USB 1.0	Low Speed (LS)	1.5 Mbit/s = 187.5 kByte/s	1.5 MByte/s NRZI-Code with Bit-Stuffing
USB 1.0	Full Speed (FS)	12 Mbit/s = 1.5 Mbit/s	12 Mbit/s NRZI-Code with Bit-Stuffing
USB 2.0	High Speed (HS)	480 Mbit/s = 60 MByte/s	480 Mbit/s NRZI-Code with Bit-Stuffing
USB 3.0	Super Speed	4000 Mbit/s = 500 MByte/s	5000 Mbit/s 8b10b-Code
USB 3.1	Super Speed +	9697 Mbit/s = 1212 MByte/s	10000 Mbit/s 128b132b-Code
USB 3.2	Super Speed +	2 lane operation with Type-C connector operation; doubling of effective data rate	

USB 1.0 and USB 2.0 use a non-return-to-zero-inverted (NRZI) coding. Typically, NRZI coding, which is also referred to as NRZ coding, follows a simple rule:

state 0: toggle | state 1: constant

When this method is applied, the polarity of a connecting wire pair in a cable has no impact on the bit sequence. This is an advantage because a change in polarity represents a 0 state, regardless of the transition direction. Figure 74 shows the schematic of the logic required for the hardware implementation of an NRZI encoder. The input signal is fed to an inverted input of an Exclusive-Or (XOR) gate. The XOR gate is a digital logic gate that gives a true (1 or high state) output whenever exactly one of the inputs has a 1-state. If both inputs are 1, or both are 0, the output equals false (0 or low state).

Behind the XOR gate, a flip-flop samples the output of the gate by the system clock. The output of the flip-flop represents the output of the coder. It feeds back into the XOR gate; as second input signal for this gate.

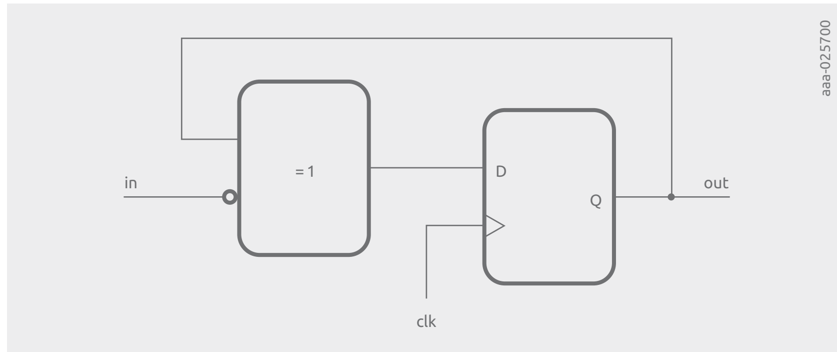


Figure 74 | NRZI(S) encoder schematic

In Table 12 an exemplary bit stream is encoded by the NRZI coder. The second row of the Table is the inverted input bit stream. The third row shows the output of the XOR. In the fourth row the coded output signal is depicted. The output bit stream shows the desired logic of a polarity toggle, which is created by a logical 0 in the input stream — with no change in the output stage for a logical 1 in the input data stream.

Table 12: Example for the NRZI(S) encoding

input	1	0	0	0	1	1	1	0	1	0	1	1	0
inverted input	0	1	1	1	0	0	0	1	0	1	0	0	1
output XOR	0	1	0	1	1	1	1	0	0	1	1	1	0
Encoder output	0	0	1	0	1	1	1	1	0	0	1	1	1

Figure 75 shows a simplified schematic of a decoder for an NRZI data stream, which detects a signal change with an output as logical state 0 and no signal change as logical state 1.

The function is realized by an XOR gate, where the data stream is connected to one input and the second input is connected to the output of a flip flop which provides the prior state of the encoder. Finally, the output of the XOR is inverted to derive the correct polarity.

Table 13 shows how the decoder works, showing the bit stream at the input in the first row, the output of the flip-flop, the output of the XOR gate before the inversion and the final output of the decoder in the last row. It is shown that the output stream of the decoding stage is identical with the input stream of Table 12.

Please note that in signal transmission it is preferable to have a DC-free system. Consequently, it is not required to have a direct galvanic connection for cable transmission between transmitter and receiver. The frequency band of the data channel does not need to start at 0 Hz but can be designed to a higher value. This ensures that data transmission can operate within a smaller frequency band.

Whenever a 0-state is transmitted, NRZI coding ensures that changes are incurred on the data during transmission. If a constant high occurs the signal can get stuck, with no oscillations occurring. For this reason, a signal change has to be forced after 6 bits in high state, which is applicable to all USB standards. Note also that seven subsequent high states indicate a bit sequence error.

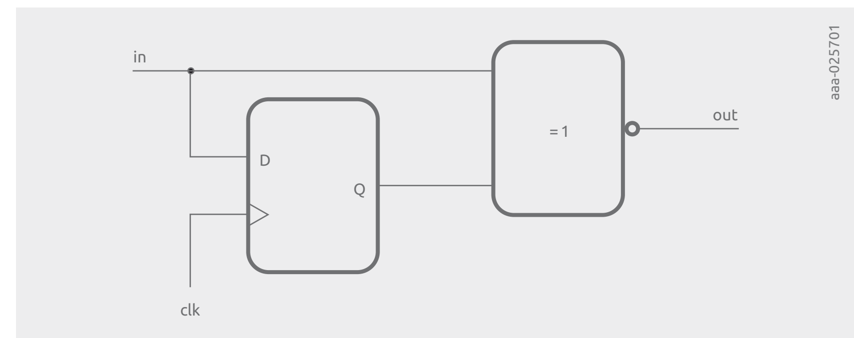


Figure 75 | Decoder schematic

Table 13: Example for NRZ decoding

input to decoder	0	0	1	0	1	1	1	1	0	0	1	1	1
output of flip-flop	x	0	0	1	0	1	1	1	1	0	0	1	1
output XOR	x	0	1	1	1	0	0	0	1	0	1	0	0
output decoder	x	1	0	0	0	1	1	1	0	1	0	1	1

Whenever D+ signal is in low state and D– is in high state, the USB bus data line state is called K-state. J-state describes the opposite condition, at which D+ is in high state and D– at in low state. Whenever both signal lines are pulled low, the system is in single-ended zero condition, referred to as SE0.

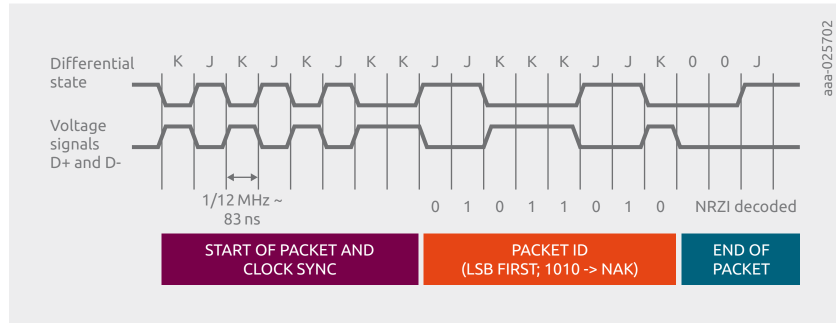


Figure 76 | Example data stream on USB 1.1 full-speed interface

Figure 76 shows a brief data stream example that transmits a NAK (Not AcKnowledged) packet at a bit rate of 12 Mbit/s, via USB 1.1 full-speed. NAK indicates that data cannot be read out (e.g. because of problems with the receiving and/or sending device/s).

Whenever real data content is transmitted, data packets are placed between the packet ID and the end-of-packet (EOP) block. The last placement of the sequence is implemented with two SE0 states, which is then followed by one idle J-state. Data transmission begins with an idle J-state: With a *00000001* sequence, i.e. with a *KJKJKJKK* sequence.

In USB 2.0 high-speed mode, the start sequence is 32 bits long, which provides more transitions. Thus, enabling the clock recovery phase-locked loop (PLL) circuit to synchronize in exact correspondence to the timing of the bit stream.

When no device is connected, the host pulls low both signal lines to ground via a 15 kΩ pull-down resistor. If a USB device is connected, one of the signal lines is pulled high via a 1.5 kΩ resistor and overwrites the pull-down state of the host.

USB 1.x speed is determined whenever D+ or D– line is pulled high via the 1.5 kΩ USB pull-up resistor. J-state signifies the idle state for USB full-speed mode; K-state signifies low-speed. A reset to SE0 condition occurs when both signal lines are pulled low by the host for 10 to 20 ms. If a USB 2.0 ready device is connected, the above described procedure for USB 1.1 devices is performed initially, but then continued with another process.

After reset, the device puts a k-state on the bus telling the host that it can handle the higher speed. After this the host toggles 3 times between J and K state to tell the USB device that the host can also support the high-speed data rate. This handshaking procedure for the speed capability of host and device is known as 'chirping' in USB literature.

9.1.2 USB 2.0 eye diagrams

The USB standard specification defines four measurement planes that are used to test a USB interface, as depicted in Figure 77. TP1 connects directly to the signal lines of the transceiver of the hub circuit board. TP2 connects the USB cable. TP3 is located directly at the input connection point of the USB device. TP4 connects directly to the pins of the receiving block of the device circuit board.

In an eye diagram measurement, an oscilloscope shows the bit transitions of a data path as an overlay of many single traces with random data content. The oscilloscope is triggered with a recovered bit clock signal because no separate clock signal is provided on an extra signal line. A data clock recovery PLL provides the data sampling clock, synchronized to data transitions.

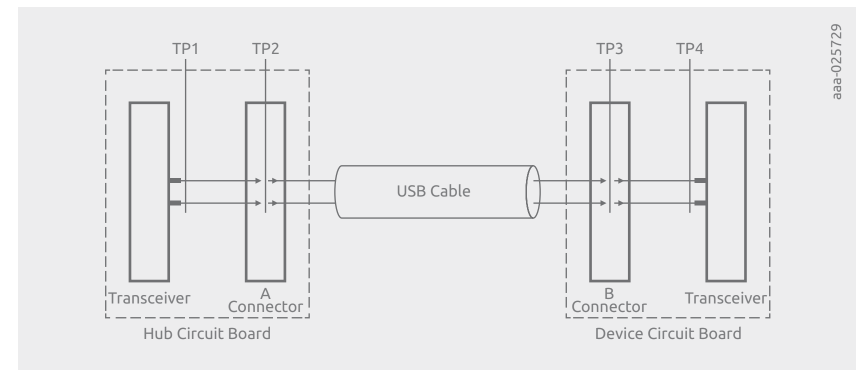


Figure 77 | Measurement planes for eye diagrams

The data eye diagram is a methodology that helps to analyze the signal quality of a high speed digital signal. Ideally, an eye diagram with a binary signal shows a row of rectangular boxes. However, in real scenarios the rise and fall times are not zero but are extended both by parasitic capacitances in the data path and by the limited speed of the transmitter stages.

Reflections, overlay of noise and jitter of the PLL clock, render a graph with a smaller open temporal window, the part of the eye diagram where no signal transitions occur. Data transitions are not located at exactly n times the symbol length. Jitter can have both a random distribution and a deterministic distribution, depending on its root cause. The nature of the jitter can be analyzed with a histogram. The width of the complete histogram represents the peak-to-peak jitter.

Figure 78 shows how the waveforms of transmitted data for a hub, measured at TP2, or for a device, measured at TP3, should look like. In a standard-compliant scenario, no signal traces are noticeable within the inner mask of the diagram, which is defined by points 1 to 6, as listed in Table 14. Each of these points is defined by a certain voltage and time within the unit interval. The unit interval is equal to the symbol length.

USB high speed shows:

$$T_{symbol} = 1/f_{symbol} = 1/480\,\text{MHz} = 2.0833\,\text{ns}$$

The temporal location is listed as a percentage value of the unit interval in the table. The nominal voltage swing of USB 2.0 is 400 mV to −400 mV. The diagram shows a second mask, which limits the signal in terms of higher voltages. The maximum voltage for the signal is ±475 mV, for a time at which no transitions occur. The voltage limit at transitions is ±525 mV, which allows some room for over- and under-shoots.

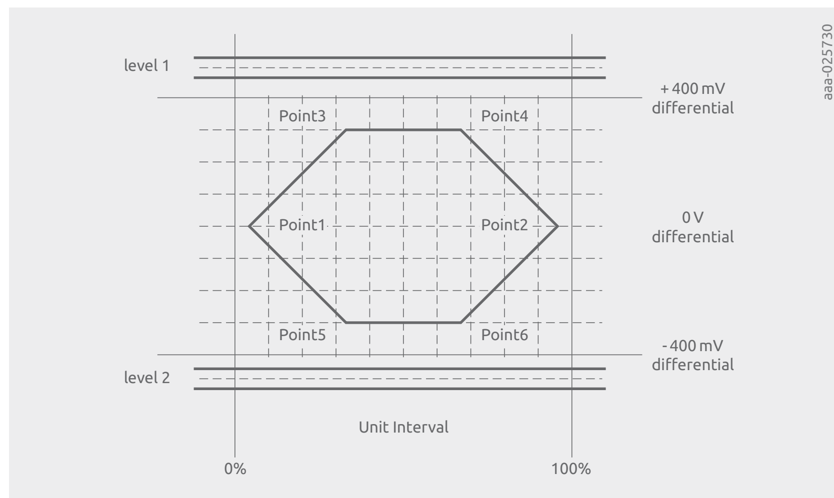


Figure 78 | Transmit waveform requirement for a hub (TP2) or a device (TP3) without a captive cable

Table 14: Parameters for the USB 2.0 transmitter eye for the test case according to Figure 76

	Voltage level (D+, D−)	Time (% of Unit Interval) 1/480 MHz = 2.0833 ns nominal
Level 1	525 mV in UI following a transition, 475 mV in all others	–
Level 2	−525 mV in UI following a transition, −475 mV in all others	–
Point 1	0V	5%
Point 2	0V	95%
Point 3	300 mV	35%
Point 4	300 mV	65%
Point 5	−300 mV	35%
Point 6	−300 mV	65%

Figure 79 shows a receiver waveform requirement scheme for a signal applied to TP4/device transceiver or to TP1/hub transceiver. The receiver mask is typically smaller than the transmitter mask, as stated above. The height of the eye is 300 mV, with a −150 mV to +150 mV range. The width of the eye is reduced to 60% of the unit interval.

Table 15 contains the details for the keep-out area for this particular test condition, which shows the smaller inner mask, as well as the upper and lower boundaries as outside limitation for the D+ and D− signal waveforms.

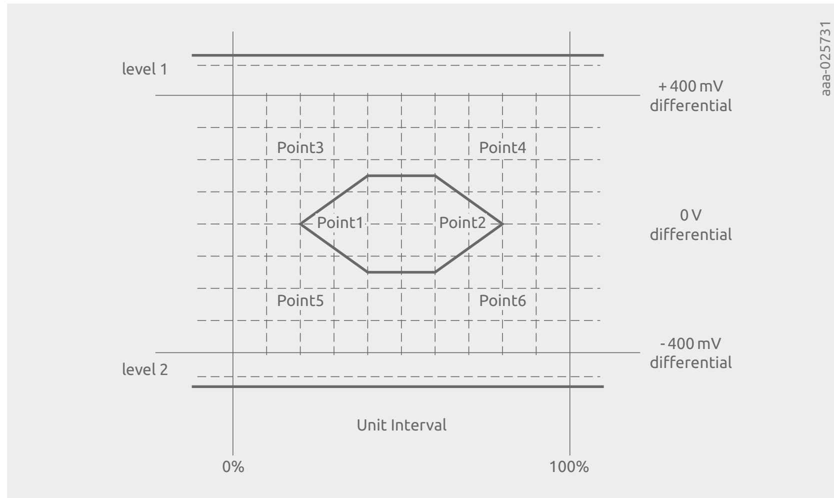


Figure 79 | Receiver waveform requirements for USB 2.0 with a signal applied at TP4 for a device transceiver or a hub transceiver with a signal applied at TP1

Table 15: Parameters for the USB 2.0 receiver eye

	Voltage level (D+, D−)	Time (% of Unit Interval) 1/480 MHz = 2.0833 ns nominal
Level 1	575 mV	–
Level 2	−575 mV	–
Point 1	0 V	20%
Point 2	0 V	80%
Point 3	150 mV	40%
Point 4	150 mV	60%
Point 5	−150 mV	40%
Point 6	−150 mV	60%

9.1.3 USB 3.0 and USB 3.1 interfaces

USB 3.0 and USB 3.1 use a different DC content removal method on signal lines, which is referred to as 8b10b-coding: 8-bit data is replaced by 10-bit data. Thus, redundancy is added to obtain both a DC-free bit stream and a limited disparity of transmitted 0-states and 1-states. In a row of 20 bits, the counts of the two possible states shall never differ by more than ±2.

Please note that after several 8b10b code words, the signal is completely DC-free. Thus, the number of ones and zeros is identical. The 8-bit original data is split into 5 bits, which are coded in 6 bits with a 5b6b-code. The remaining 3 bits are coded in 4 bits with a 3b4b-code. Thus, forming the final 8b10b-coding scheme.

The coding operates on a running disparity (RD): After each symbol, the count of ones and zeros differs either by 1 or −1. Table 13 lists the RD coding rules. For clarification, two processes based on the rules in Table 16, are explained:

- If a code word has a disparity of zero, no disparity change occurs for the next coded word.
- If a code word has a disparity option +/− 2, a disparity is selected that prompts a sign change for the next word. To achieve this, there must be two coding options for words, which do not have an equal number of zeros and ones.

Table 16: Rules for Running Disparity coding

Previous RD	Disparity of Code word	Disparity chosen	Next RD
−1	0	0	−1
−1	+/− 2	+2	+1
+1	0	0	+1
+1	+/− 2	−2	−1

Table 17: 5b6b code table

Input	EDCBA	RD = −1	abcdei	RD = +1
D.00	00000	100111		011000
D.01	00001	011101		100010
D.02	00010	101101		010010
D.03	00011		110001	
D.04	00100	110101		001010
D.05	00101		101001	
D.06	00110		011001	
D.07	00111	111000		000111
D.08	01000	111001		000110
D.09	01001		100101	
D.10	01010		010101	
D.11	01011		110100	
D.12	01100		001101	
D.13	01101		101100	
D.14	01110		011100	
D.15	01111	010111		101000
D.16	10000	011011		100100
D.17	10001		100011	
D.18	10010		010011	
D.19	10011		110010	
D.20	10100		001011	
D.21	10101		101010	
D.22	10110		011010	
D.23	10111	111010		000101
D.24	11000	110011		001100
D.25	11001		100110	
D.26	11010		010110	
D.27	11011	101110		001001
D.28	11100		001110	
D.29	11101	101110		001110
D.30	11110	011110		100001
D.31	11111	101011		010100

Table 17 above shows how the original 5-bit code words are coded into 6-bit code words. Each new 6-bit code word contains either:

- 3 zeros and ones
- 2 ones and 4 zeros
- 4 zeros and 2 ones

The 6-bit code word in column RD = +1 can be created easily by inverting all bits of the code word in column RD = −1.

Table 18 below is the coding scheme from 3-bit to 4-bit.

Table 18: 3b4b-code table

Input	HGF	RD = −1	fghj	RD = +1
D.x.0	000	1011		0100
D.x.1	001		1001	
Dx.2	010		0101	
D.x.3	011	1100		0011
D.x.4	100	1101		0010
D.x.5	101		1010	
D.x.6	110		0110	
D.x.P7	111	1110		0001
D.x.A7	111	0111		1000

Please note that Table 17 and 18 each contain one exception to the rule. The word codes *111000* (RD = –1) and respectively *000111* (RD = +1) in Table 17 (*EDCBA* column value *00111*) each contain the same number of zeros and ones. The same applies for the word codes *0011* and *1100* in Table 18 (*HGF* column value *011*).

High-speed interfaces like PCI Express, Serial ATA, Display Port, Fibre Channel Gigabit, Ethernet and DVB make use of 8b10b-coding, which also supports AC-coupling. This makes clock recovery much easier. Clock recovery with a PLL clock generator is required in all scenarios in which no separate clock signal is sent with the data. The PLL of the data receiver needs to synchronize to the data signal transitions to allow safe sampling of incoming data.

USB high-speed, and the slower modes, make use of one differential pair with signal lines D+ and D– for data transmission, which allows half duplex data transmission. USB 3.x makes use of two differential pairs. This allows data flow in both directions in full duplex mode.

Figure 80 shows the termination of the D+ and D– lines. On both sides of the connection a 45 Ω single-ended termination to ground is implemented. This results in a 90 Ω differential termination of the signal lines. In practice, the 45 Ω serial resistor behind the LS/HS drivers are switched to ground. By doing so, the serial resistor functions as 45 Ω termination for this high-speed use case.

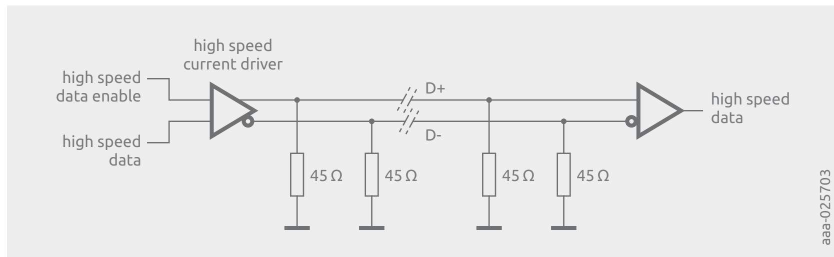


Figure 80 | Basic termination scheme for USB HS-Mode

The high-speed drivers are implemented as switched current sources that deliver 17.78 mA in single-ended high state. Figure 81 shows this basic driver structure. The high state voltage at the 45 Ω resistors in parallel operation is:

$$V_{SEhigh} = \frac{17.78\ mA}{22.5\ \Omega} = 400\ mV$$

The nominal differential voltage swing on the D+/D– signal pair is therefore ±400 mV.

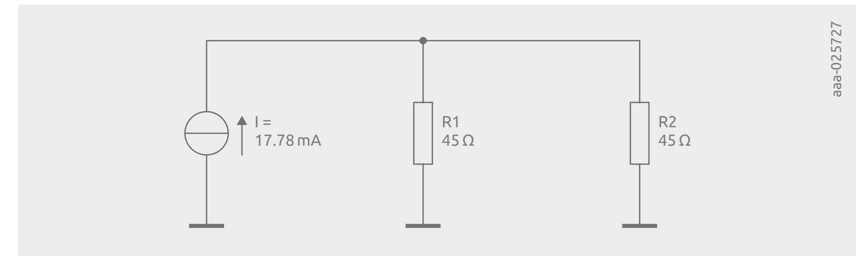
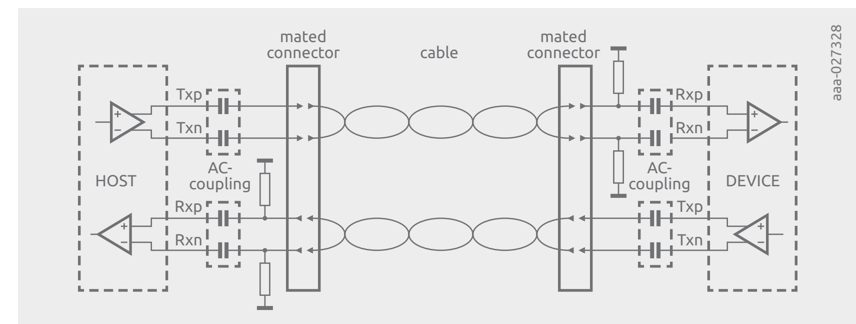


Figure 81 | HS 17.78 mA current source attached to each signal line (D+/D–)

In Figure 82 the coupling of the two differential signal pairs for the super speed signals RX and TX is depicted. At every transmitter side, the TX lines contain capacitors that realize AC-coupling for both differential connection lanes. The nominal capacitance of these capacitors is 100 nF. The figure shows the cable connection of a host and a USB device that is plugged into mated connectors.

Currently, it is practice to place additional 330 nF capacitors at the data inputs RXp and RXn and a 250 kΩ termination to ground at the cable side of the capacitors as an extension of the USB 3 standard.



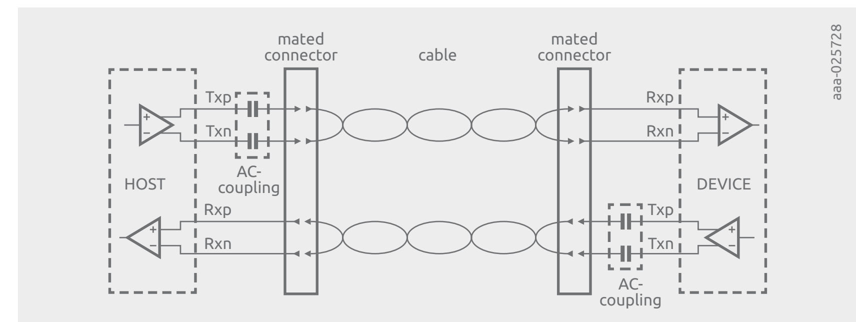


Figure 82 | Rx and Tx connection scheme for USB 3

9.1.4 USB 3.0 eye diagrams

If a connection is set up via a USB 3 Gen 1 or USB Gen 2 connection, a link training is performed as sequence, with the following steps:

1. Configuring and initializing of link
2. Bit-lock and symbol lock
3. Rx equalization training
4. Lane polarity inversion
5. Block alignment (USB Gen 2 only)

Training sequences are always 8b10b coded and not scrambled. Table 19 shows the most important normative requirements for USB 3 Gen 1 and Gen 2 transmitters.

Table 19: Basic requirements for the USB 3 transmitter

Symbol	Explanation	Gen 1, 5 Gbit/s	Gen 2, 10 Gbit/s
UI	Unit Interval	199.94 ps (min) 200 ps (nom) 200.06 ps (max)	99.97 ps (min) 100 ps (nom) 100.03 ps (max)
$V_{TX\text{-}Diff\text{-}PP}$	Differential peak to peak TX voltage swing	0.8 V (min) 1 V (nom) 1.2 V (max)	0.8 V (min) 1 V (nom) 1.2 V (max)
$V_{TX\text{-}DE_RATIO}$	TX de-emphasis	3dB (min) 4dB (max)	3-tap FIR equalizer
$R_{TX\text{-}DIFF\text{-}DC}$	DC differential impedance	72 Ω (min) 90 Ω (nom) 120 Ω (max)	72 Ω (min) 90 Ω (nom) 120 Ω (max)
$C_{AC\text{-}COUPLING}$	AC coupling capacitor	75nF – 200nF	75nF – 265nF
$T_{TX\text{-}EYE}$	Transmitter eye width	0.625 UI (incl. all jitter sources)	0.625 UI (incl. all jitter sources)

Table 20 is the equivalent list for the receiver side of the super-speed USB interface. The minimum height of the receiver eye is quite low. The open width is also much smaller compared to USB super-speed.

Table 20: Basic requirements for the USB 3 receiver

Symbol	Explanation	Gen 1, 5 Gbit/s	Gen 2, 10 Gbit/s
UI	Unit Interval	199.94 ps (min) 200 ps (nom) 200.06 (max)	99.97 ps (min) 100 ps (nom) 100.03 ps (max)
$V_{RX\text{-}DIFF\text{-}PP\text{-}POST\text{-}EQ}$	Differential peak to peak RX voltage swing	100mV (min)	70mV (min)
RX equalizer	receiver equalizer	0dB – 6dB	0dB – 6dB
T_j	total jitter	0.66 unit intervals	0.714 unit intervals
$R_{RX\text{-}DIFF\text{-}DC}$	DC differential impedance	72 Ω (min) 90 Ω (nom) 120 Ω (max)	72 Ω (min) 90 Ω (nom) 120 Ω (max)
$C_{AC\text{-}COUPLING}$	AC coupling capacitor	75nF – 200nF	75nF – 265nF

Figure 83 shows the receiver mask for 5 Gbit/s, and Figure 84 depicts the related mask for 10 Gbit/s. The mask in the USB 3 Gen 1 scenario has a minimum eye height of 100 mV whereas the eye height in USB 3 Gen 2 scenario is only 70 mV. The minimum eye width is 0.34 unit intervals, respectively 0.286 unit intervals, in the 10 Gbit/s scenario. Moreover, the shape of the mask is also different. In the 5 Gbit/s scenario the mask has the shape of a rhombus whereas the shape in the 10 Gbit/s scenario is like the USB 2.0 scenario, with a 0.1-unit interval width for the upper and lower mask borders.

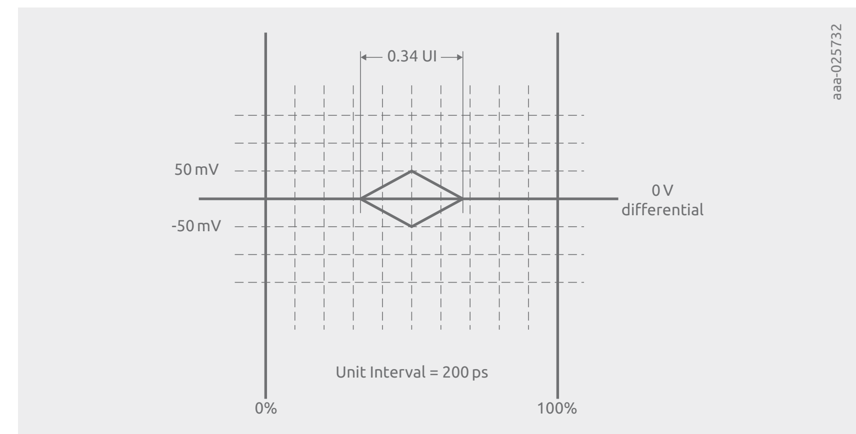


Figure 83 | Mask diagram of USB 3 Gen 1 scenario (5 Gbit/s)

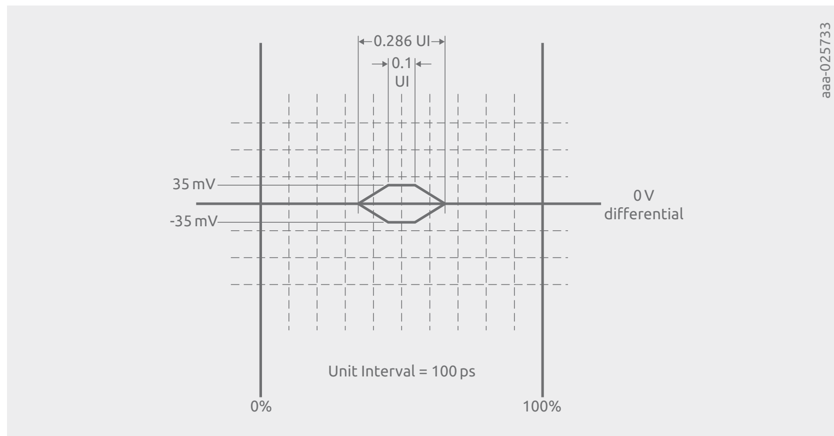


Figure 84 | Mask diagram of USB 3 Gen 1 scenario (10 Gbit/s)

9.1.5 USB Type-C

The user-friendly 24-pin connector allows reversible plugs. The innovative connector type supports up to USB 3 Gen 2 speed at 10 Gbit/s, as well as USB 2.0 power delivery. For a further data speed increase of a factor 2, USB 3.2 introduces 2 lanes for RX and TX running in parallel. Full-feature cables are electronically marked with an identification IC. Alternate modes can be set up via the dedicated configuration channels, with vendor defined messages (VDMs).

The Type-C connector can support various other standards beside USB. They are Display Port, Thunderbolt 3, MHL, PCI Express and Base-T Ethernet. Various dongles that convert from USB Type-C to legacy connectors or other interface standards like HDMI are available on the market.

In Table 21 the pin assignment of USB Type-C connector is listed. Figure 85 shows a front view of a Type-C plug. The 24 pins are organized in two groups of 12 pins each, i.e. group A and group B. Pins are available for four differential pairs with Super Speed operation (two lanes each for RX_P/RX_N and TX_p/TX_n). Moreover, two pins for USB 2.0 lane pair (Dp/Dn), two configuration channel pins (CC1 and CC2) and two sideband usage (SBU) pins. Additionally, 4 GND and 4 V_{BUS} pins that ensure low resistance for the power path.

Table 21: USB Type-C pin assignment

Pin number	Signal name	Explanation
A1	GND	Ground
A2	SSTXp1	Super Speed differential TX pair 1, positive signal
A3	SSTXn1	Super Speed differential TX pair 1, negative signal
A4	V_{BUS}	Bus Power line
A5	CC1	Configuration Channel 1
A6	Dp1	USB 2.0 differential pair 1, positive signal
A7	Dn1	USB 2.0 differential pair 1, negative signal
A8	SBU1	Sideband Usage signal 1
A9	V_{BUS}	Bus Power line
A10	SSRXn2	Super Speed differential RX pair 2, negative signal
A11	SSRXp2	Super Speed differential RX pair 2, positive signal
A12	GND	Ground
B1	GND	Ground
B2	SSTXp2	Super Speed differential TX pair 2, positive signal
B3	SSTXn2	Super Speed differential TX pair 2, negative signal
B4	V_{BUS}	Bus Power line
B5	CC2	Configuration Channel 2
B6	Dp2	USB 2 differential pair 2, positive signal
B7	Dn2	USB 2 differential pair 2, negative signal
B8	SBU2	Sideband Usage signal 2
B9	V_{BUS}	Bus Power line
B10	SSRXn1	Super Speed differential RX pair 1, negative signal
B11	SSRXp1	Super Speed differential RX pair 1, positive signal
B12	GND	Ground

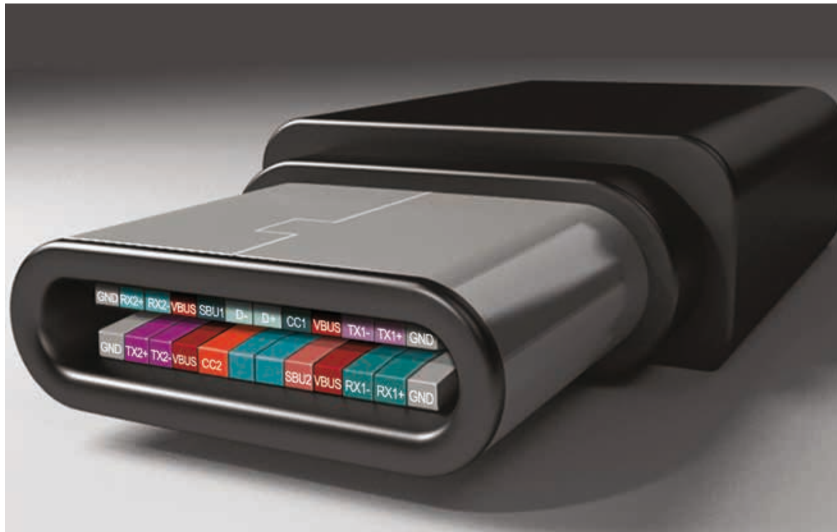


Figure 85 | Pinout and front view of USB Type-C connector

As soon as the connection is established, the orientation of the cable connection is detected via the CC pins. The Type-C cable has one physical CC wire only. With this single connection both ends of the cable can detect the appropriate super-speed lines needed for data exchange:

For example, the connection process of a downstream facing port (DFP) to an upstream facing port (UFP) occurs, as follows:

1. DFP to UFP attach/detach detection
2. Plus orientation/cable twist detection
3. Initial DFP-to-UFP (host to device) and power relationship detection
4. USB Type-C VBUS current detection and usage
5. USB power delivery (PD) communication
6. Discovery and configuration of functional extensions

Figure 86 depicts a DFP to UFP connection scenario. On the DFP side, pull-up resistors Rp are implemented towards a positive supply voltage. On the other end of the cable pull-down resistors are connected to ground.

Please note that as default, a current source can be configured instead of using RP pull-up resistors. The node with the higher voltage of the two

CC pins indicates the direction of the connection. Ra is available for powered cables and audio adapters, as shown in Table 24 below. The Rp value can detect 5 V-current capability.

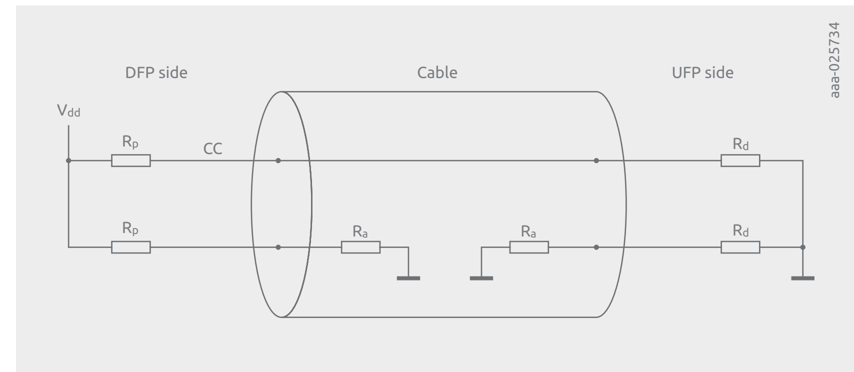


Figure 86 | DFP-UFP CC model connection

In Table 22 the value for the pull-up resistor Rp and the related power rating is shown for either a 5 V or 3.3 V supply connected to the pull-up as supply voltage. Alternatively, the standard also allows the use of a current source instead of pull-up resistors.

Table 23 defines how the pull-down resistor Rd is specified. The nominal termination is a 5 kΩ resistor. Voltage clamping does not allow detection of power capability. For this function the tolerance of Rd needs to be ±10% at least.

Table 22: Down-stream port (DFP) Rp requirements

DFP Dedication	Current Source to 1.7 V – 5.5 V	Pull-up resistor to 4.75 V – 5.5 V	Pull-up resistor to 3.135 V – 3.465 V
Default USB power	80 µA +/– 20%	56 k +/– 20%	36 +/– 20%
1.5 A/5 V	180 µA +/– 8%	22 k +/– 5%	12 +/– 5%
3.0 A/5 V	330 µA +/– 8%	10 k +/– 5%	4.7k +/– 5%

Table 23: Up-stream port (UFP) Rd requirements

Rd implementation	Nominal value	Power detection capability	maximum voltage at the CC pin
+/– 20% voltage clamp	1.1 V	no	1.32 V
+/– 20% resistor to GND	5.1 kΩ	no	2.18 V
+/– 10% resistor to GND	5.1 kΩ	yes	2.04 V

The Ra termination resistor has a nominal resistance of 1 kΩ, as shown in Figure 86. It is often applied via a JFET that limits the current after detection process, as shown in Figure 87.

As soon as the pitch-off voltage of the depletion FET is reached, the current increases the voltage level in Ra at the source of the depletion FET until it clamps the current to a maximum value. Thus, power loss is reduced whenever the 5 V supply voltage Vconn is switched to the CC line.

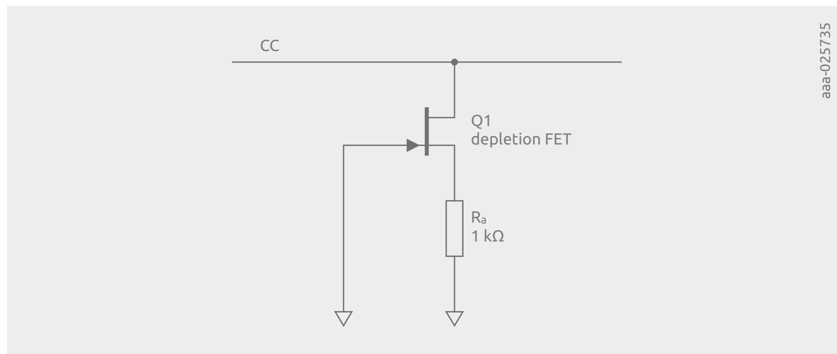


Figure 87 | R_a termination solution

Table 24 is a list of states that result from CC line termination in a DFP-UFP connection.

Table 24: CC connection model for a DFP-UFP scenario

CC1	CC2	State
open	open	Nothing attached
Rd	open	UFP attached
open	Rd	UFP attached
Ra	open	Powered cable, no UFP attached
open	Ra	Powered cable, no UFP attached
Ra	Rd	Powered cable and UFP attached
Rd	Ra	Powered cable and UFP attached
Rd	Rd	Debug accessory Mode attached
Ra	Ra	Audio adapter accessory Mode attached

9.2 HDMI interfaces

HDMI is a digital interface in consumer and computing applications. In automotive, HDMI is sometimes used to connect headrest displays or dash cams. It is similar to DVI but also includes consumer electronics control (CEC). Video data is transmitted without data compression whereas audio can be used with or without data compression.

The interface is HDCP copy-protected. High-speed data is transmitted via transition minimized differential signaling (TMDS) lines. The interface uses three TMDS lanes and one additional channel for the clock signal.

As of HDMI 1.4, HDMI also supports an ethernet data channel on the HEC lane. The display data channel (DDC), that is similar to I²C, is used to exchange information. The resolution compatibility is supported whenever an HDMI connection is established. Thus, extended display identification data (EDID) can be read out.

9.2.1 Contact assignment for connectors

In Table 25 the contact assignments for Type A connectors, which are the most commonly used connectors in TVs, monitors, DVD players and computers, are listed. Figure 87 shows an HDMI connector front view. Type D micro-HDMI connectors are used for tablets, cameras and other mobile devices.

Table 25: Contact assignment for HDMI Type A and Type C connector

Contact Type A	Contact Type D	Signal description
Pin 1	Pin 3	TMDS Data2+
Pin 2	Pin 4	TMDS Data2 shielding
Pin 3	Pin 5	TMDS Data2–
Pin 4	Pin 6	TMDS Data1+
Pin 5	Pin 7	TMDS Data1 shielding
Pin 6	Pin 8	TMDS Data1–
Pin 7	Pin 9	TMDS Data0+
Pin 8	Pin 10	TMDS Data0 shielding
Pin 9	Pin 11	TMDS Data0–

Contact Type A	Contact Type D	Signal description
Pin 10	Pin 12	TMDS clock+
Pin 11	Pin 13	TMDS clock shielding
Pin 12	Pin 14	TMDS clock–
Pin 13	Pin 15	CEC
Pin 14	Pin 2	reserved (HDMI1.0–1.3), HEC data– (HDMI 1.4)
Pin 15	Pin 17	DDC clock (I²C-Bus, SCL)
Pin 16	Pin 18	DDC data (I²C-Bus, SDA)
Pin 17	Pin 16	Ground for DDC, CEC and HEC
Pin 18	Pin 19	−5 V supply with 55 mA maximum current
Pin 19	Pin 1	Hot-Plug-Detection (all standards), HEC Data+ (HDMI 1.4)

Figure 88 | Pinout and front view of HDMI connector

9.2.2 HDMI key parameters connection structure

HDMI introduced consecutively additional standards with higher data rates that are necessary for high resolution displays. Table 26 shows a brief overview of HDMI versions and contains maximum pixel rates, as well as maximum clock rates and TMDS bit rates. The Table also lists maximum screen resolutions for consumer applications and supported maximum color depths of the pixels. TMDS lines have a ratio between clock and bit rate of factor 10 for HDMI 1.4, and factor 14 for HDMI 2.0.

Table 26: List of HDMI key parameters for the different versions

HDMI version	1.0	1.1	1.2	1.3	1.4	2.0	2.1
Maximum pixel clock rate (MHz)	165	165	165	340	340	600	no extra clock channel
Maximum TMDS bit rate per lane including 8b/10b coding overhead (Gbit/s)	1.65	1.65	1.65	3.4	3.4	6	12
Maximum total TMDS throughput including 8B/10b coding overhead (Gbit/s)	4.95	4.95	4.95	10.2	10.2	18	48
Maximum audio throughput bit rate (Mbit/s)	36.86	36.86	36.86	36.86	36.86	49.152	49.152
Maximum video resolution over 24 bit/pixel single link	1920* 1200 p/ 60 Hz	1920* 1200 p/ 60 Hz	1920* 1200 p/ 60Hz	2560* 1600 p/ 60 Hz	4096* 2160 p/ 30 Hz	4096* 2160 p/ 60 Hz	7680* 4320 p/ 60 Hz
Maximum color depth (bit/pixel)	24	24	24	48	48	48	48

Figure 89 shows the basic HDMI TMDS data connection structure of transmitters and sink connectors. The transmitter has a switched current source of 10 mA. A differential signal connection with matched impedance builds the data path to the receiver. The receiver terminates each signal line of the differential interface with 50 Ω to a 3.3 V supply line.

This leads to a single-ended nominal voltage swing of:

$$V_{SE} = 10\,mA \cdot 50\,\Omega = 500\,mV$$

Consequently, the nominal differential voltage swing is 1 V, which is twice the value of a single-ended data line. The differential nominal termination is 100 Ω, which is twice the value of the single-ended pull-up resistors of the HDMI sink connectors. The impedance matching must be kept in an 85 Ω to 115 Ω window, i.e. 100 Ω ±15%; to comply with HDMI specification.

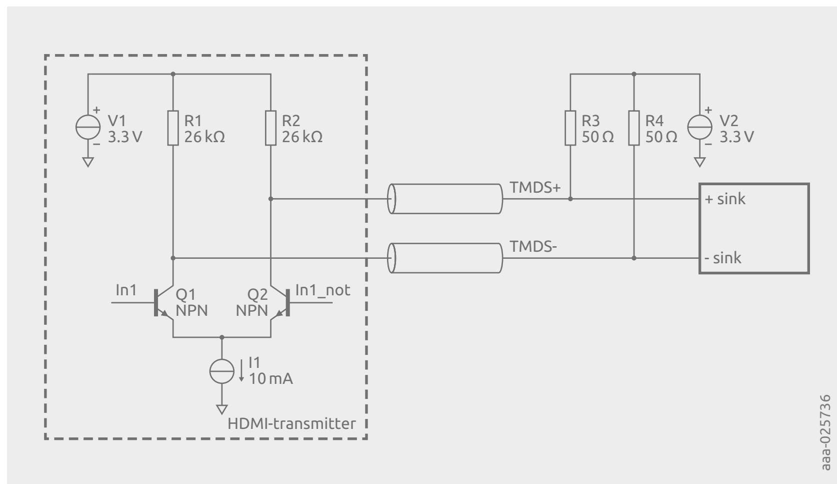


Figure 89 | Structure of a HDMI transmitter to receiver driver

Figure 90 shows the HDMI 1.4 transmitter mask, as well as upper and lower limits of the TMDS line voltage. The eye has a minimum height of 400 mV, and a width of 0.7 unit intervals.

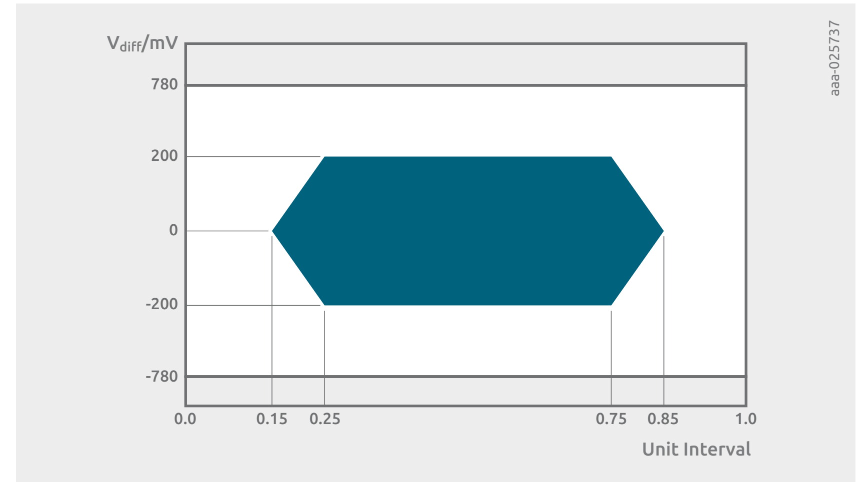


Figure 90 | Eye diagramm mask of a HDMI 1.4 transmitter

Figure 91 depicts the HDMI 1.4 receiver mask. Eye height is 300 mV (±50 mV) and eye width has to be at minimum 50% of the unit interval.

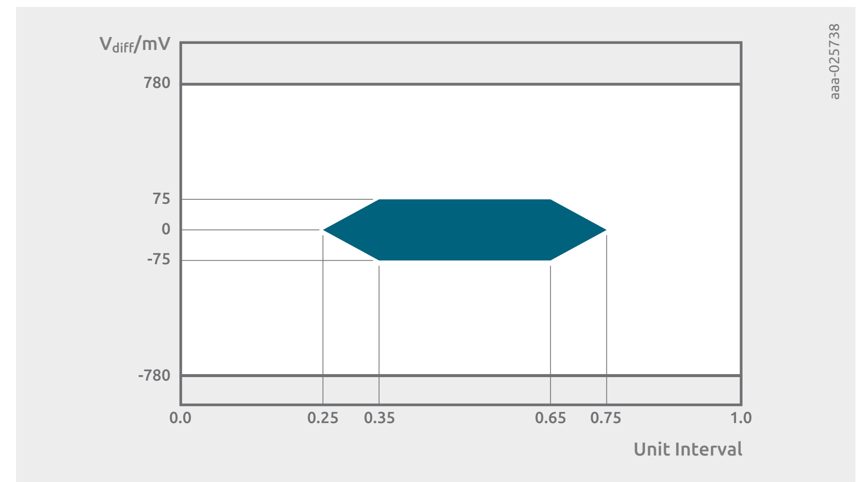


Figure 91 | Eye diagramm mask of a HDMI 1.4 receiver

Figure 92 shows the set-up of eye diagrams for eye diagram measurements with HDMI 2.0 at the source test points. TP1 is located on the receptacle plug of the pattern generator, with the test point adapter (TPA). A cable emulator based on worst-case conditions is placed between TPA-P and reference cable equalizer, followed by the TP1_EQ.

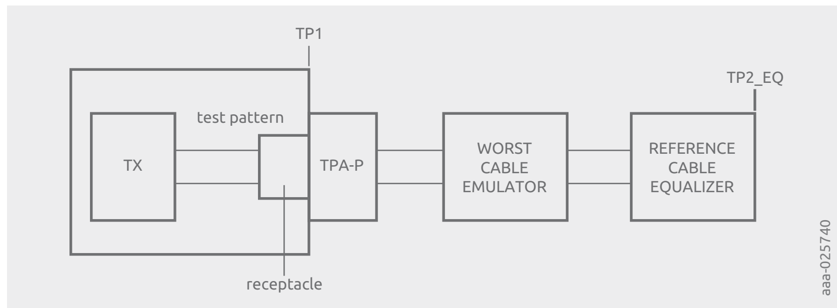


Figure 92 | HDMI Source Test point for eye diagram measurement

Figure 93 depicts the HDMI 2.0 mask diagram for test point TP2_EQ. Eye height H and eye width V depend on the HDMI bit rate, as shown in Table 27. To achieve the maximum bit rate of 6 Gbit/s, a minimum eye height of 150 mV and a maximum data jitter of 0.6 unit intervals are necessary; with total data jitter $T_j = 1 - H$.

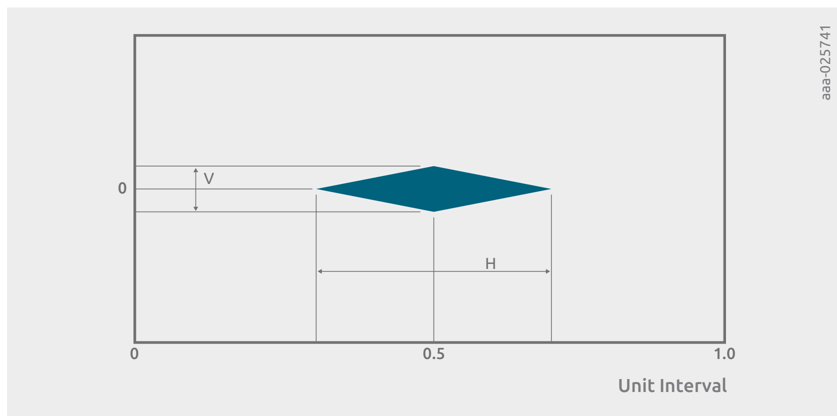


Figure 93 | HDMI2.0 mask for eye diagram measurements

Table 27: Mask size in dependency of the Bit Rate (Gbit/s)

TMDS Bit Rate (Gbit/s)	Mask width H (UI)	mask height V (mV)
3.4 < bit rate ≤ 3.712	0.6	335
3.712 < bit rate ≤ 5.94	−0.0332 * (bit rate)² + 0.2312 * (bit rate) + 0.1998	−19.66 * (bit rate)² + 106.74 * (bit rate) + 209.58
5.94 < bit rate ≤ 6.0	0.4	150

9.3 MIPI interface

The MIPI Alliance comprises several companies that define a data communication standard for interfacing processor and chip-sets to peripheral components such as cameras, sensors and displays. Application areas include mobile devices like smartphones, tablets and embedded systems like TVs. In automotive, MIPI is common for camera applications. However, many of the MIPI specifications are already used or adapted for automotive applications [34].

Although most MIPI interfaces are not normally used for external interfaces with direct access for users, ESD protection is applied to safeguard against ESD strikes entering a device via housing gaps or in case of an opened cover. Major key facts for the physical layer of MIPI standards D-PHY, M-PHY and C-PHY are discussed in the following chapters. The recently announced A-PHY specification is described briefly in Section 8.4 as it is a SerDes interface.

9.3.1 MIPI D-PHY

MIPI D-PHY [35] is a synchronous connection between a master and slave, and the master provides the clock signal as a unidirectional signal. One or more data lanes can be used for data transmission. The minimum configuration consists of two differential signal connections or lanes, so one clock lane and at least one data lane. The direction of data flow can be unidirectional and bidirectional. Data flow direction is indicated by an exchange of token in half-duplex mode. The data speed in reverse direction is a fourth of forward direction.

A low voltage level signal is transmitted in High-Speed mode transferring data in a burst mode. A so-called Low-Power Signaling mode is foreseen for transmission of control commands. The specification does not mention a fixed maximum data rate per lane, but indicates a range from 80 to 1500 Mbit/s. If a higher data rate is required, the number of differential data pairs has to be increased.

Figure 94 shows an example for the line levels on a signal line of MIPI D-PHY. The red part of the signal shows a High-Speed data burst, whereas the blue part shows a Low-Power signaling event.

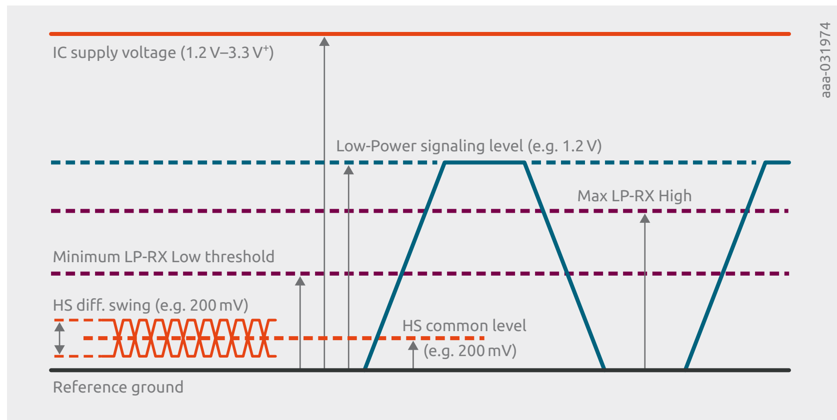


Figure 94 | Line levels for MIPI D-PHY

In Table 28 the lane states are listed. A data lane can operate in either High-Speed mode or Low-Power mode. High speed data transmission starts and stops with Stop state LP-11, which is a single ended high-state on both lines of the differential pair.

The sequence to be sent for High-Speed operation is LP-11 (stop), LP-01 (high speed request), LP-00 (bridge), and the interface stays in High-Speed mode until a stop command is received. The Control Mode is the default condition of the interface, while Escape Modes can be entered via a request sent in Control Mode.

Table 28: List of lane states for MIPI D-PHY

State Code	Line Voltage Levels		High-Speed	Low Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	not applicable	not applicable
HS-1	HS High	HS Low	Differential-1	not applicable	not applicable
LP-00	LP Low	LP Low	not applicable	Bridge	Space
LP-01	LP Low	LP High	not applicable	HS-Request	Mark-0
LP-10	LP High	LP Low	not applicable	LS-Request	Mark-1
LP-11	LP High	LP High	not applicable	Stop	not applicable

On the transmitter side, the maximum output voltage in high state VOH in Low-Power mode is 1.3 V, while the minimum level for the low state VOL is −50 mV as depicted in Table 29.

Table 29: Transmitter DC characteristics for Low-Power Mode

Parameter	Description	min	nominal	max
V_{OH}	output level high-state	1.1 V	1.2 V	1.3 V
V_{OL}	output level low-state	−50 mV	0 mV	50 mV

On the receiver side, the minimum input voltage in logical high-state VIH in Low-Power mode is 880 mV. The input level for the logical low-state has to stay below 330 mV, as Table 30 shows.

Table 30: Receiver DC characteristics for Low-Power Mode

Parameter	Description	min	nominal	max
V_{IH}	input level high-state	880 mV	–	–
V_{IL}	input level low-state	–	–	300 mV

Table 31 lists the most important transmitter DC characteristics. The differential lines have a nominal common mode voltage of 200 mV overlaid with the HS signal of 100 mV single-ended swing, which means 200 mV nominal differential swing amplitude.

Table 31: High-Speed transmitter DC characteristics

Parameter	Description	min	nominal	max
V_{CMTX}	HS transmitter static common mode voltage	150 mV	200 mV	250 mV
$\|V_{DD}\|$	HS transmitter differential voltage	140 mV	200 mV	270 mV
V_{OHHS}	HS output high-level voltage	–	–	360 mV
Z_{OS}	single ended output resistance	40 Ω	50 Ω	62.5 Ω
ΔZ_{OS}	single ended output resistance mismatch	–	–	10%

On the receiver side, at least +/– 70 mV are required to exceed the thresholds for the differential voltage for logical high or low state as depicted in Table 32.

Table 32: High-Speed receiver DC characteristics

Parameter	Description	min	nominal	max
V_{CMRX}	Common mode voltage HS receive mode	70 mV	–	330 mV
V_{IDTH}	Differential input high state threshold	–	–	70 mV
V_{IDTL}	Differential input low state threshold	−70 mV	–	–
V_{IHHS}	Single-ended input high voltage	–	–	460 mV
V_{ILHS}	Single-ended input low voltage	−40 mV	–	–
Z_{ID}	Differential input impedance	80 Ω	100 Ω	125 Ω

9.3.2 MIPI M-PHY

MIPI M-PHY [36] is the successor of the MIPI D-PHY standard. It addresses the growing demand for higher data rates per lane, better power efficiency and more flexibility. It uses a synchronous connection between a master and slave. The clock signal is generated via a clock PLL, so there is no dedicated clock signal transmitted from a master as with D-PHY interfaces.

Figure 95 gives an example of a MIPI M-PHY interface in which unidirectional lanes are used as data connections. Every lane connects an M-TX transmitter block to an MN-RX receiver block. For higher data rates several lanes can be foreseen in both directions.

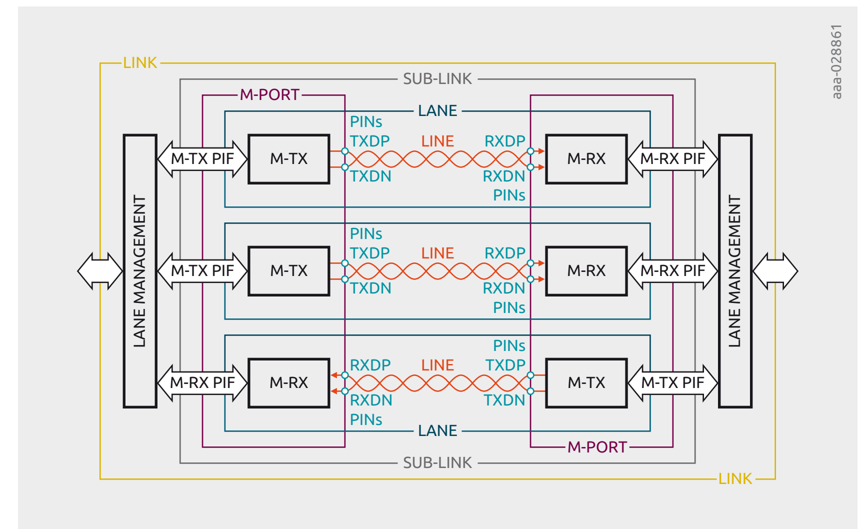


Figure 95 | MIPI M-PHY example for lane structure

Data are transmitted in the so-called HS-Burst state in HS-Mode encoded in 8b10b and put on the signals lines in a NRZ signaling. There are two series defined with related data rates that are denoted as a GEAR for each couple. The different supported data rates are listed in Table 33. shows a brief overview of HDMI versions and contains maximum pixel rates, as well as maximum clock rates and TMDS bit rates. The Table also lists maximum screen resolutions for consumer applications, and support

Table 33: High-Speed burst data rate, M-PHY series and GEARs

Rate A-series (Mbit/s)	Rate B-Series (Mbit/s)	High-Speed GEARs
1248	1457.6	HS-G1 (A/B)
2496	2915.2	HS-G2 (A/B)
4992	5830.4	HS-G3 (A/B)
9984	11680.8	HS-G4 (A/B)

Figure 96 shows the termination scheme of MIPI M-PHY. The TX drivers switch one of the differential lines to ground and the other line to V_{LD} depending on the differential lane state. Each driver output has a serial resistor R_{SE_TX} connected to the outgoing signal line. 40 Ω is the minimum value for R_{SE_TX}, the maximum allowed value is 60 Ω. The receiver side RX only requires a termination in the High-Speed Mode (HS Mode).

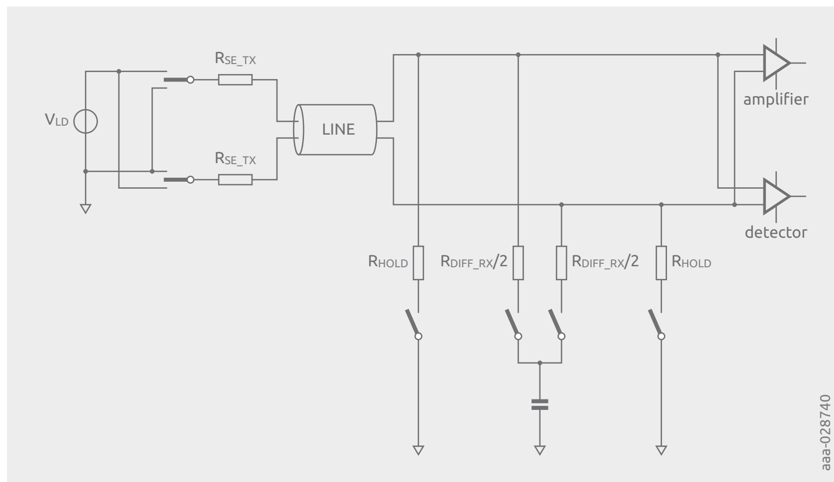


Figure 96 | MIPI M-PHY termination scheme

Figure 97 shows the transmitter side MIPI M-PHY eye diagram for the High-Speed mode in GEAR 3 and GEAR 4. The minimum eye height is 80 mV. The temporal eye width has to be 0.55 unit intervals in GEAR 3 and 0.5 unit intervals in GEAR 4. These key parameters are listed in Table 34.

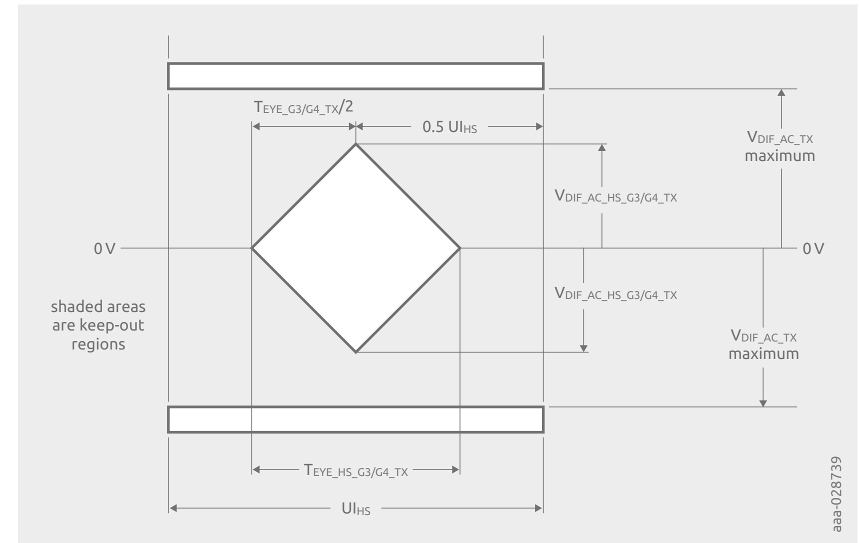


Figure 97 | M-PHY TX eye diagram for HS-Mode GEAR 3and 4

Table 34: High-Speed GEAR 3 and GEAR 4 electrical TX key parameters

Parameter	Value	Description
$V_{DIF_AC_HS_G3/4_TX}$	40 mV, minimum	Differential TX AC voltage in HS-G3/4
$V_{DIF_AC_HS_G4_TX}$	40 mV, minimum	Differential TX AC voltage in HS-G4
$T_{EYE_HS_G3_TX}$	0.55 Unit intervals (UI)	Transmitter eye opening in HS-G3
$T_{EYE_HS_G4_TX}$	0.5 Unit intervals (UI)	Transmitter eye opening in HS-G4

The receiver side eye diagram looks like the transmitter side diagram. For the highest data speed of MIPI M-PHY HS-Speed GEAR 4, the height of the eye is the same as the transmitter eye height. It is twice $V_{DIF_AC_HS}$, equal to 40 mV as minimum requirement. The open eye width $T_{EYE_HS_G4_RX}$ is defined as 1 — TJ_{RX} measured in unit intervals. TJ_{RX} is lower or equal to 0.52 unit intervals for GEAR 4. This means that the open eye is 0.48 unit intervals wide in temporal direction as minimum requirement.

9.3.3 MIPI C-PHY

MIPI C-PHY [37] uses three signal lines instead of two lines for conventional differential data lanes. This allows a higher data rate without needing 4 signal lines for two parallel standard differential lanes. MIPI C-PHY achieves 2.28 bits per symbol. It has some similarities with MIPI D-PHY for the transition between low power modes and high-speed modes. Unlike the D-PHY standard, no separate clock channel is provided. The combination of signal voltages on the lines changes from symbol to symbol. This makes it comparatively simple to regenerate the clock signal because of transitions after each symbol.

The maximum symbol rate is 3 GSps (Giga symbols per second). This symbol rate is the relevant value for the frequency spectrum to be considered for the selection of ESD protection devices. 1.5 GHz is the highest frequency of the fundamental wave in high speed mode.

Table 35 shows the signal voltages for the signal lines A, B and C in the columns wire amplitude, the receiver differential input voltages A-B, B-C and C-A, and the related digital output stages in the left three columns. The line voltages are all combinations of 0.25 V, 0.5 V and 0.75 V for the three wires. The corresponding 3 voltage differences have a sum of zero for every state +x, −x, +y, −y, +z or −z. A positive difference corresponds to a digital high state for the digital output of the receiver.

Table 35: Signal voltage and differential voltages for the six C-PHY lane states

Wire State	Wire Amplitude			Receiver differential input voltage			Receiver digital output		
	A	B	C	A-B	B-C	C-A	Rx-AB	RX-BC	RX-CA
+x	3/4 V	1/4 V	1/2 V	+1/2 V	−1/4 V	−1/4 V	1	0	0
−x	1/4 V	3/4 V	1/2 V	−1/2 V	+1/4 V	+1/4 V	0	1	1
+y	1/2 V	3/4 V	1/4 V	−1/4 V	+1/2 V	−1/4 V	0	1	0
−y	1/2 V	1/4 V	3/4 V	+1/4 V	−1/2 V	+1/4 V	1	0	1
+z	1/4 V	1/2 V	3/4 V	−1/4 V	−1/4 V	+1/2 V	0	0	1
−z	3/4 V	1/2 V	1/4 V	+1/4 V	+1/4 V	−1/2 V	1	1	0

Figure 98 shows how the six lane states are realized to achieve the voltages for the signal lines according to Table 35. At the transmitter side the lines can be switched to the driver voltage V+ or ground via a 50 Ω termination via a pull-up (PU) or pull-down (PD) switching FET. Together with the receiver termination of 2 × 50 Ω between the two comparator inputs, the voltage levels +/− 1/4 V and +/− 3/4 V are generated. For example, in the line state +x, the driver voltage +V is switched to the A line via a 50 Ω resistor by the switch PU_A. The positive input of the comparator RX_AB is connected to a divider created by this 50 Ω PU and the 100 Ω between the comparator inputs plus the PD resistor of 50 Ω from the switch PD_B connected to ground. This results in the 3/4 +V level on the A signal wire. A second stage with 100 Ω PU and PD resistors and switching FETs create the 1/2 +V voltage for a signal line. This can be seen for example in state +x for the C signal wire.

If +V is connected to line A (via PU_A) and the switch to ground is active at line B (PD_B), the state +x is called A to B as well. For the opposite polarities the state −x can be nominated B to A. The corresponding receiver, RX_AB in the example discussed, the receiver difference is either +1/2 +V or −1/2 +V. This is the background for so-called positive or negative polarity like the left and right separation in Figure 97. For the second row with the two y states the same system can be applied for the wires B and C and the polarity is reflected in the polarity of the differences at the inputs of RX_BC.

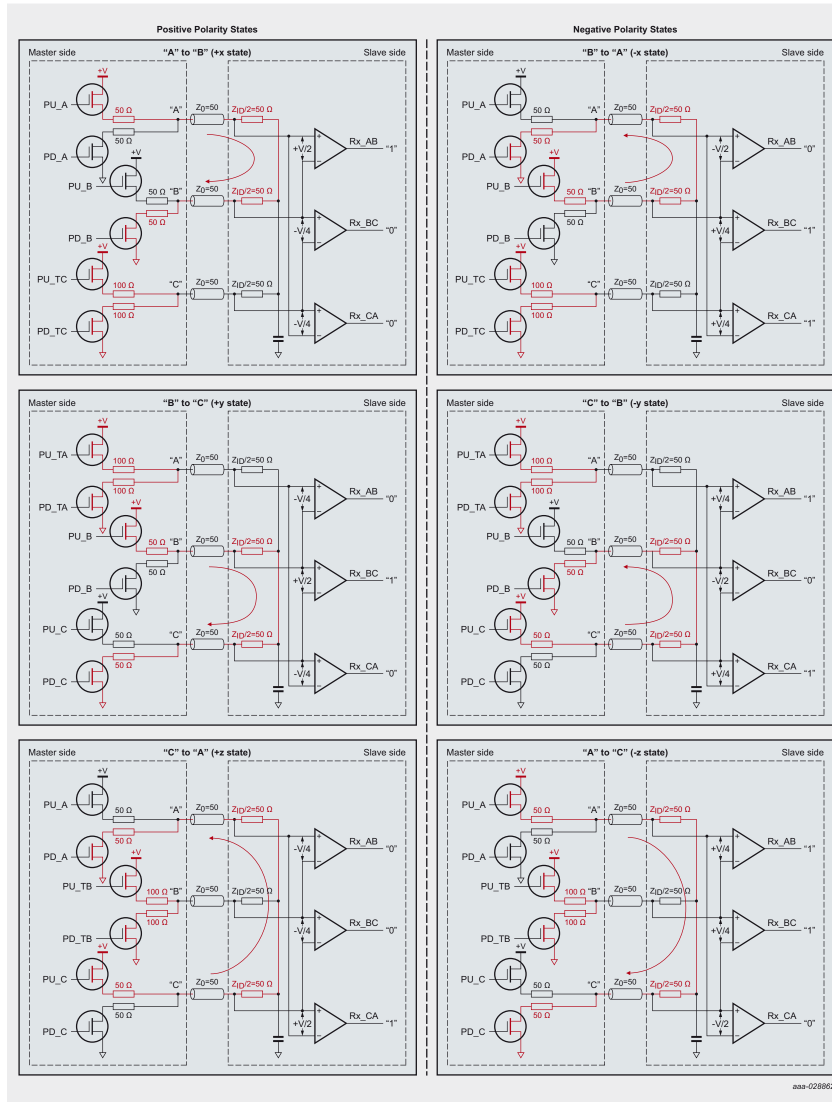


Figure 98 | The six C-PHY wire states in nominal condition, with driver and receiver side structure

From the six possible states there are five possible transitions to any other state. These transitions are depicted in Figure 99. Like in Figure 98 the states are divided in positive and negative polarities in the inner circle and the negative states outside the inner circle.

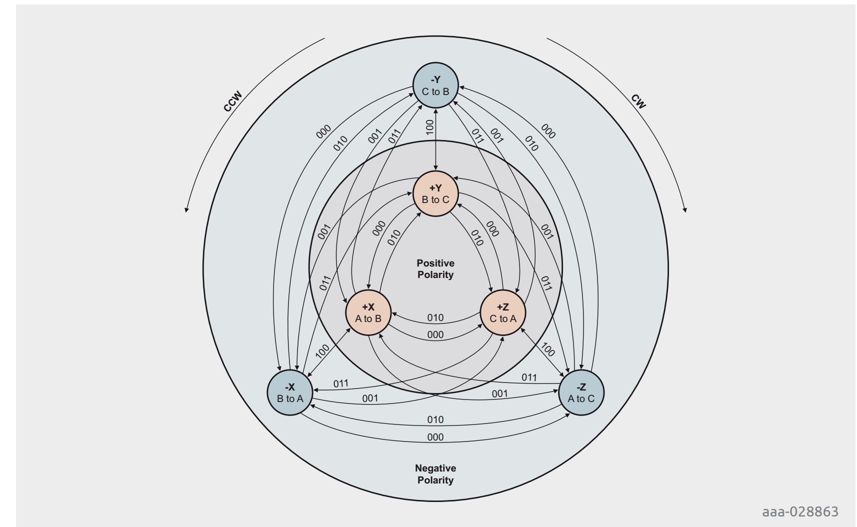


Figure 99 | All six MIPI states with all possible five transitions

Each transmitted symbol is represented by a 3-bit number for the transitions between the six wire states with the values 000, 001, 010, 011 and 100. These values can be found in blue at the transition arrows. C-PHY defines three state change parameters which are flip, rotate and polarity, represented in the three bits of the transition values.

The least significant bit indicates a polarity change, so a change from light grey area to dark grey or the opposite direction in the diagram. The next significant bit indicated the direction of rotation in the diagram for the wire state. If it is clockwise (CW in diagram) the bit is set to 1, in the counter-clock direction (CCW) it is 0. Finally, the most significant bit stands for a flip of the same state in polarity. This is, for example, a change from state +x to –x or vice versa. The flip transitions are represented with the value 100. Polarity change and rotation bits are put to zero.

Table 36 shows all five transitions with the symbol values in the left column from every wire state in time interval N-1 to any other present state. The right column indicates which facts can be assigned to each transition in terms of direction of rotation and polarity change, as well as the flip case, indicated also as same phase in the C-PHY standard.

Table 36: Transitions from previous state to present state

Symbol Input Value	Previous Wire state, interval N-1 +x	−x	+y	−y	+z	−z	description of transition facts
000	+z	−z	+x	−x	+y	−y	Rotate CCW, pol. is the same
001	−z	+z	−x	+x	−y	+y	Rotate CCW, pol. is opposite
010	+y	−y	+z	−z	+x	−x	Rotate CW, pol. is the same
011	−y	+y	−z	+z	−x	+x	Rotate CW, pol. is opposite
1xx	−x	+x	−y	+y	−z	+z	same phase, pol. is opposite

Figure 100 shows a receiver eye diagram for MIPI C-PHY in high speed mode. The height of the eye has to be at least 80 mV which is twice V_{IDTH} threshold voltages for the differential receivers. The eye width $T_{EYE_WIDTH_RX}$ is at least 0.5 unit intervals.

The maximum signal voltage on a line can be 1.35 V which is related to LP mode.

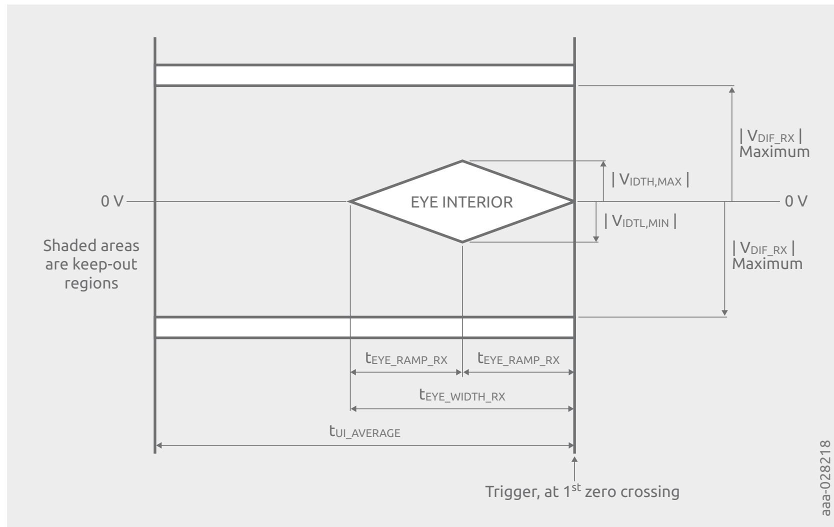


Figure 100 | High speed mode receiver eye diagram for MIPI C-PHY

Figure 101 gives an example of an eye measurement at a C-PHY interface. The signal shows the voltage levels 'Strong 0' and 'Strong 1' as well as 'Weak 0' and 'Weak 1' as to be expected from Table 35. The test scope is triggered at the right side zero crossing behind the open eye.

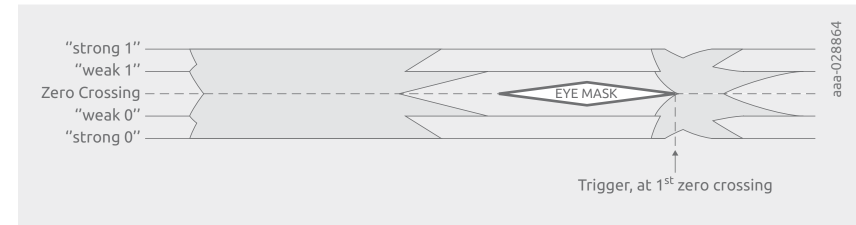


Figure 101 | Eye diagram measurement MIPI C-PHY

9.4 Antenna interfaces

RF antennas are the interface between electromagnetic waves and electrical current. Independent of whether the antenna is receiving or transmitting, any component that is added to the antenna system should not interfere with the signal, to maintain the optimum transmission or reception performance. In automotive applications, antennas are encountered in various places. Very common nowadays are NFC, digital radio, 5G, and GPS. Additionally, antenna for keyless entry and V2X communication are present.

If an antenna is removable or if there is a need for factory programming and tuning, antenna connectors are used. These connectors give ESD discharges an entry point into the system. Even though antennas may sometimes seem completely hidden, there are still numerous instances where internal antenna connectors are used. Such internal antenna connectors may be subject to ESD discharges during device assembly.

Figure 102 | Removable antenna

If an ESD event occurs at an antenna terminal, it can cause severe damage to the sensitive circuitry. Thus, external ESD protection is strongly recommended to achieve good ESD robustness.

Figure 102 shows an F-Connector interface for a removable antenna. Figure 103 gives an example of internal antenna contacts as an interconnect to another board that can be seen in many smartphone applications. An internal antenna terminal is illustrated in Figure 104.

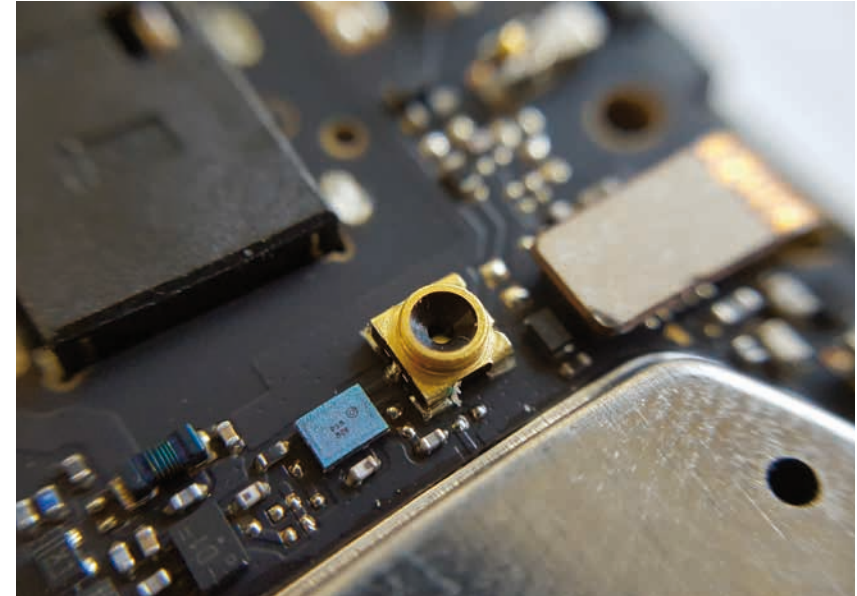


Figure 103 | Internal antenna contacts

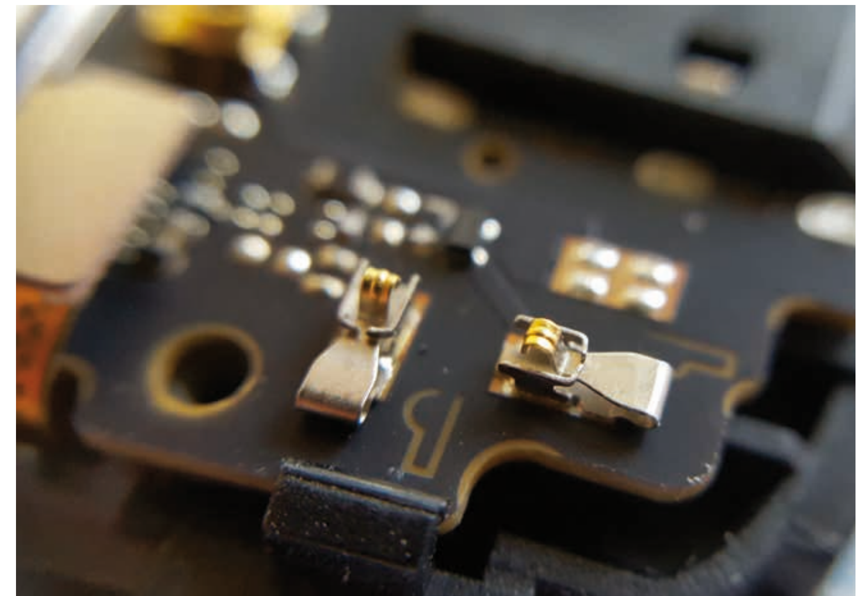


Figure 104 | Internal antenna terminal

Chapter 10

Supply line protection with TVS diodes

Transient voltage suppressors (TVS) protect connections such as signal or supply lines (but not data lines) against overvoltage. When placed on a signal or supply line connected to a sensitive component (e.g. a highly integrated SoC), harmful overvoltage can be discharged through the protection device. In contrast to external ESD protection devices, TVS protection devices can withstand significantly higher surge pulses but usually have parasitic capacitances that are too high to be put on a data line.

There are numerous sources of high current surge pulses. On the automotive board net, surge events can originate from within the board net (switching of inductive loads or ignition) or from exterior events, like coupled energy from lightning pulses. Signals and sensors are exposed to surge events from coupling of high energy pulses and from charging cables during assembly or maintenance. When modules are connected to the car and GND is not connected first, there is always a risk of a surge on the cables that are connected first. With multimedia interfaces like USB and diagnostics interfaces, surge events from charging cables are also to be expected.

The Nexperia terminology denotes a difference between ESD protection products and TVS products. Namely, TVS protection devices (or PTVS) can withstand significantly higher energy originating from high current surge pulses and are meant to be placed on supply lines. In literature often both protection devices are classified as TVS, this can also be the case with other protection device suppliers.

10.1 Pulse standards

Depending on the source of the pulse it may have different pulse shapes (i.e. pulse length and rise/fall times) and energy. Common surge pulse standards are described in Sections 3.4 and 3.5.

It is worth noting that although standards like IEC 61000-4-5 are intended to describe the direct or indirect effect of lightning strikes to power lines, devices that are tested to this standard are not subject to these events. The test methods are used to characterize device robustness against other events that contain a similar amount of energy and have similar pulse shape.

For a vehicle's board net of 12 V, ISO7637-2 and ISO16750-2 describe various pulses and conditions that need to be considered. These requirements are designed to check for ECU compliance in general. However, transient pulse tests like ISO7637-2 Pulses 1,2a,2b,3a,3b and ISO16750-2 §4.6.4 (load dump) are often applied to single TVS devices.

10.2 TVS operation

As long as the voltage on the protected line stays below the breakdown voltage of the TVS diode, it does not react. Once the voltage on the line reaches the protection device's breakdown voltage it will start conducting current to ground, resulting in the voltage being clamped to V_{CL}. Based on fundamental parameters of a TVS protection device (mainly breakdown voltage V_{br} and dynamic resistance R_{dyn} — see Chapter 2 for details), the clamping voltage for the peak current of a pulse can be calculated by

$$V_{CL} = I_{PP} \cdot R_{dyn} + V_{BR}$$

The lower voltage V_{CL} is the better the protection of the system. So a low R_{dyn} is essential for a good TVS device. Very often the total power dissipation is used as a selection criterion. However, one should be careful not to look only at this parameter, as it is linked to the clamping voltage:

$$P_{tot} = I_{PPM} \cdot V_{CL} = I^2_{PPM} \cdot R_{dyn} + I_{PPM} \cdot V_{BR}$$

A low R_{dyn}, which is desired for good protection behavior, leads to a lower P_{tot}. Instead of comparing P_{tot}. one should compare the maximal current times the breakdown voltage $I_{PPM} \cdot V_{BR}$.

10.3 Bidirectional and unidirectional TVS

Surge pulses on the automotive board net can be positive and negative, so often bidirectional devices are requested. However, in combination with a suitable reverse polarity protection, unidirectional TVS devices can be used. Figure 105 show the different operation modes for positive and negative pulses for bi- and unidirectional TVS.

The bidirectional breaks down in both directions. The unidirectional device needs to be placed behind the reverse polarity protection to comply with ISO16750-2. Positive pulses pass the reverse polarity protection and is directed to ground through the TVS. Negative pulses pass the TVS in forward direction. The reverse polarity protection blocks the voltage or goes into avalanche. Especially for low cost implementations using a pn-rectifier with a high voltage rating, a unidirection TVS is an elegant solution. But also with robust Schottky or MOSFET based reverse polarity protections, unidirection TVS are applicable. In any case, it needs to withstand or survive the worst-case negative pulse. Usually, ISO7637-2 Pulse 3a with -150 V considered.

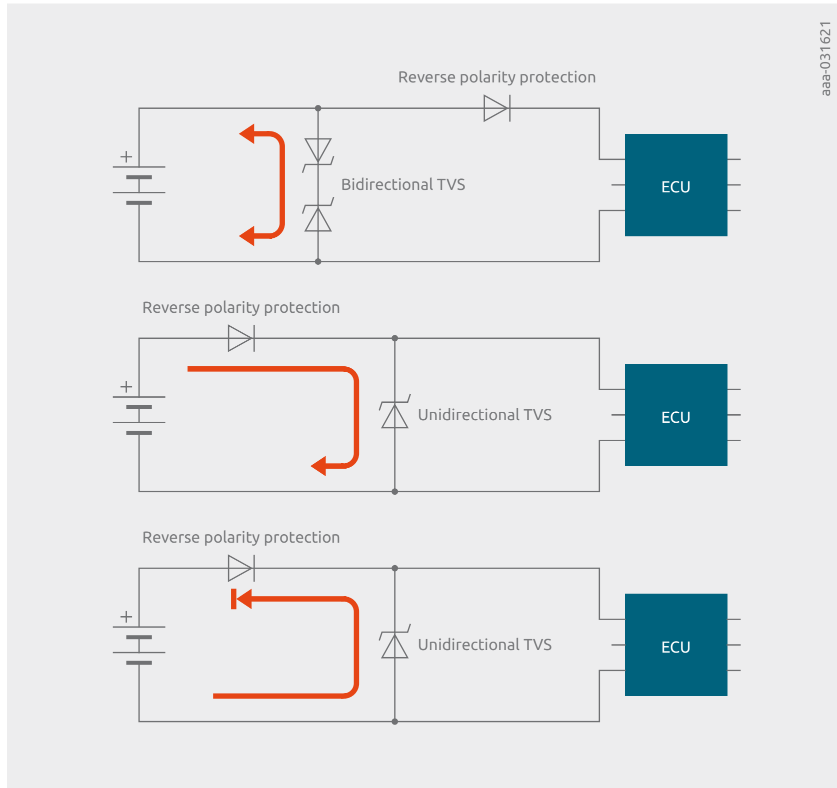


Figure 105 | Current flow for positive and negative pulses with bidirection (upper) and unidirection (mid and lower) TVS

Chapter 11

SEED – Modelling of system-level ESD events

One of the main challenges designers and manufacturers of the electronic systems face these days is to combine broad application functionality fulfilling customer needs with its sustainability in terms of electrostatic discharge (ESD) events. These events may occur in the field and lead to the system failures, resulting in short term system upsets (soft failures) or even provoke physical degradation of the system chip (SoC or IC) functionality leading to the so called hard failures.

System Efficient ESD Design (SEED) methodology can be applied to support engineers in modelling electronic systems and in simulation of their behaviour under ESD conditions. The transient system analysis can be used to predict system-level ESD robustness during the development phase and can help minimize long development cycles. This provides an opportunity to reduce expenses and time to market for new ESD protection components and system ESD protection solutions [38–42].

The challenge here is the non-availability of appropriate models for different parts of a system, which are necessary for SEED simulation. The typical system, see Figure 106, consists of an SoC or IC, which primarily should be protected against ESD. Since IC internal ESD protection circuits can provide reasonable ESD safety only during fabrication and transportation processes, an external ESD protection solution will be applied. Here we can see an external ESD component connected to the signal trace near the socket pin of the system. In this case the advantage of the signal trace parasitics as well as of the discrete components located on it can be used to improve ESD performance of the ESD device and consequently improve the overall system-level ESD robustness.

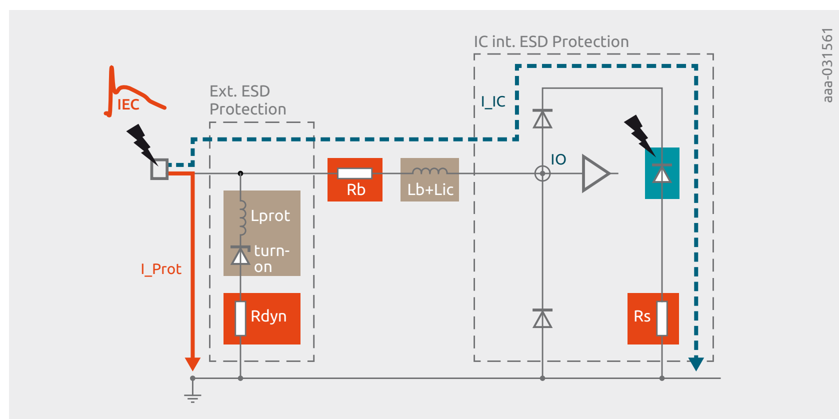


Figure 106 | A simplified example of the equivalent circuit of a system, consisting of external ESD protection component, signal trace parasitics and rail-to-rail internal ESD protection of the IC. The system dynamic and quasi-static parameters are marked with brown and orange boxes correspondingly.

Typically, two types of models will be used to realize SEED models: equivalent circuit models, for passive devices, ESD Generator or TLP models, etc.; and behavioural models to model non-linear devices or systems, concurrently avoiding description of complex physical processes. Additionally, discrete components, S-Parameter blocks or transmission line models may be added to describe characteristic of the signal line.

11.1 System failure scenarios

In case of ESD events, the external ESD protection device should be able to protect the whole system. That includes not only the system IC but also sensitive passive components placed on the signal trace. To realize that, the used protection device should be good in two aspects. It should turn-on very quickly and have as low on-resistance (also marked as dynamic resistance) as possible. Also, its parasitic inductance (due to wire-bonds and metallization contacts) should be as low as possilbe. Finally, the parameters of the ESD protection device together with the signal trace and IC internal ESD protection parameters define the ESD robustness of the whole system. We will now discuss two different failure scenarios.

Scenario 1 – very sensitive gate oxides

The first scenario describes the situation where the sensitive gate oxides of MOSFET transistors will be destroyed by voltage overshoot during the first few nanoseconds of the entering ESD pulse. The failure scenario occurs with very sensitive gate oxides. In automotive applications, this kind of failure is more likely in the multimedia and high-speed SerDes interfaces than in classic IVNs. Figure 107 shows an example where the dynamic voltage overshoot, which occurs at the I/O pin, exceeds the limit of the IC maximum allowed voltage drop. The red curve shows the corresponding voltage drop over the external ESD protection device.

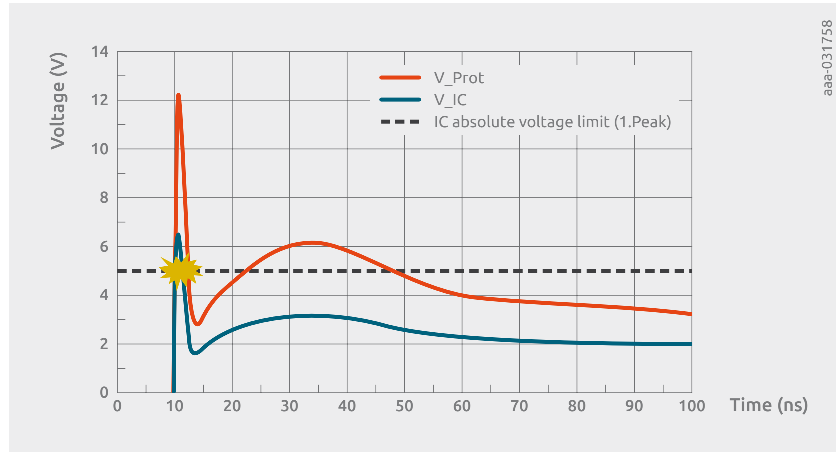


Figure 107 | Evaluation of voltage in time domain: blue curve shows the voltage overshoot at the IC internal I/O pin whereas the red curve indicates the voltage drop across the external ESD protection device, the dashed black line defines the absolute IC voltage limit

There are two factors which can influence the distribution of dynamic overshoot further into the system. The first factor is the turn-on behaviour of the external ESD protection device, also known as conductivity modulation [14] and its parasitic inductance. The second factor is the ratio of parasitic inductances in the system, forming a voltage divider Vprot/(Vtrace + Vic). Therefore, proper modelling of device or system reaction on the entering rising edge of the ESD pulse is essential for correct representation of dynamic system-level behaviour during an ESD event. Inductive behaviour can be relatively easy modelled by adding lumped elements into the simulation. However a challenge arises to model the turn-on behaviour of the external ESD protection device, especially if it is a protection device with snapback.

Scenario 2 – power dissipation inside the IC

In the second scenario the system is subjected to high power dissipation inside the IC due to the high current flow through the IC internal ESD protection components. This subsequently leads to thermal system damage referred to as EOS. In that case the ratio of the system resistances Rprot/(Rb+Rs) defines the amount of rest current which flows into the IC. Figure 108 shows the residual current inside the IC internal ESD protection (blue curve) together with the current of the external ESD protection device (red curve).

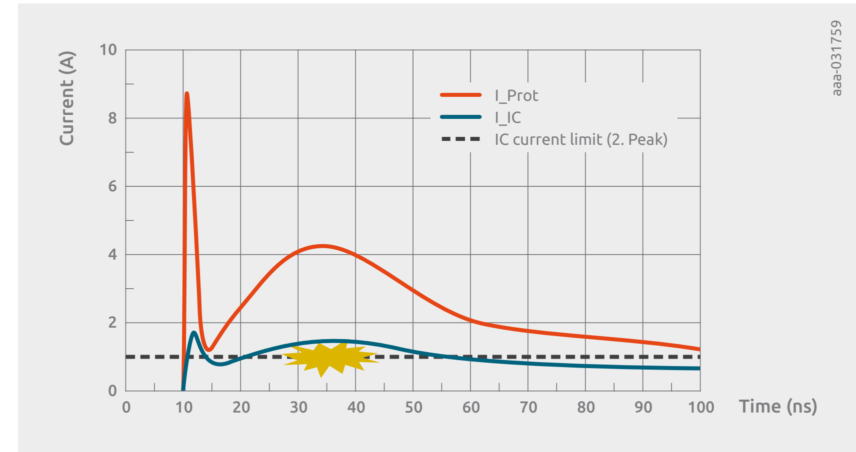


Figure 108 | Evaluation of current in time domain: blue curve shows the residual current through the IC internal ESD protection whereas the red curve indicates the current through external ESD protection device, the dashed black line defines the IC current limit in steady state condition

11.2 Modelling of ESD protection devices with snapback

For precise transient analysis of a system from perspective of both discussed failure scenarios, the SEED model of ESD protection device should encounter both quasi-static and dynamic behaviour. Two different modelling approaches will be discussed: quasi-static and dynamic.

11.2.1 Quasi-static model with snapback

Figure 109 illustrates the small-signal model, typically implemented with SPICE models, and the high current model of an external ESD protection device with snapback. The idea of the quasi-static model is to combine those into one model and extend this with the transition from trigger point Vt to Vh.

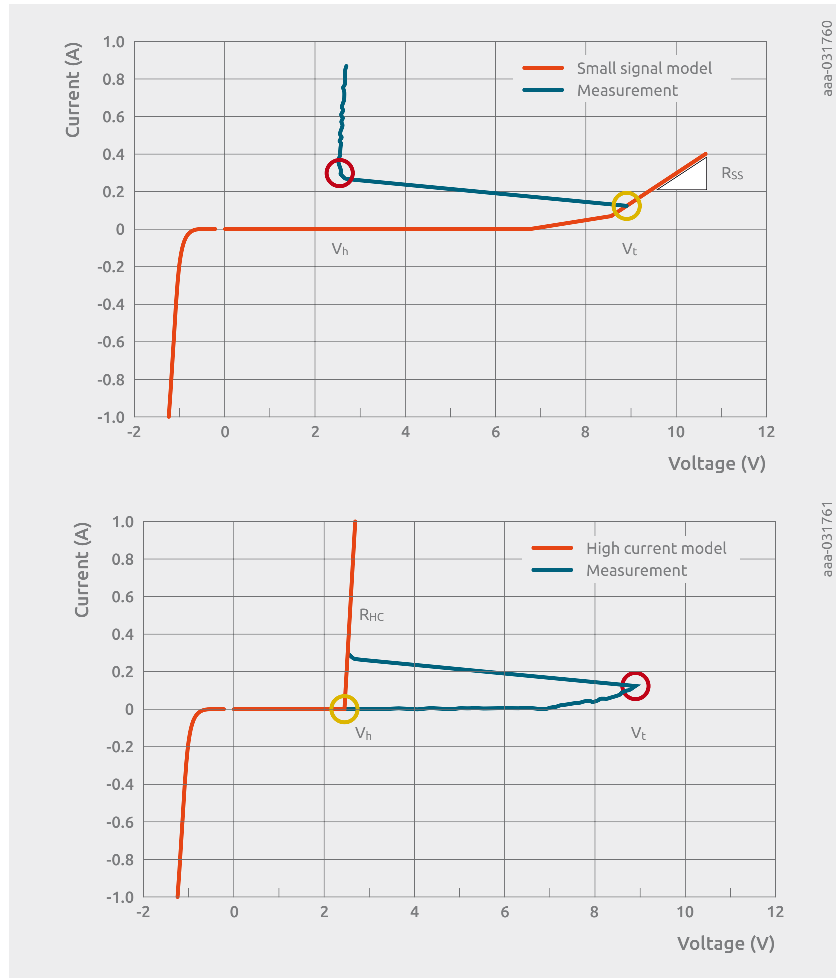


Figure 109 | The upper graphic shows the small-signal modelling results of the external ESD protection device with snapback, whereas the lower graphic illustrates the high current model

The I-V data, which is necessary to describe the quasi-static behaviour of the device can be acquired using TLP measurement method [43]. Figure 110 shows schematically how the current and voltage characteristic of the device in time domain obtained by variation of applied pulse amplitude and constant rise time can be captured.

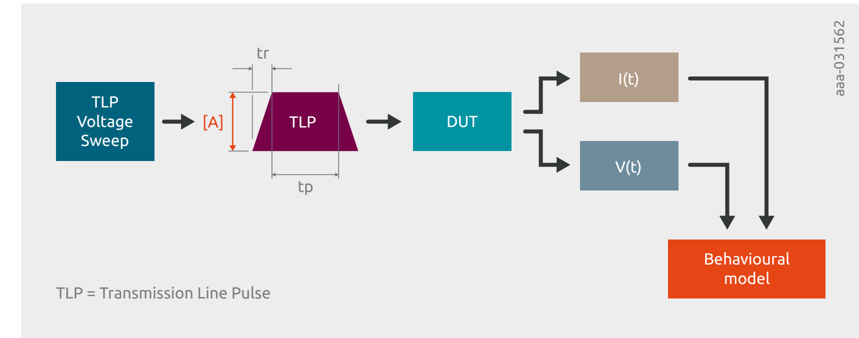


Figure 110 | Principle of acquisition of time domain I-V characteristic of the DUT using TLP measurement method to tune behavioural models of ESD protection devices

Finally, all averaged values of current and voltage time domain curves evaluated in the time window of 70 ns to 90 ns will be put together to describe I-V characteristic of the DUT. The extracted I-V curve can be then used as basis for tuning of quasi-static and dynamic behavioural models of ESD protection components.

Implementation in VerilogA

VerilogA is a well-known hardware programming language for analog circuits that uses a reduced instruction set from Verilog-AMS (Analog Mixed Signal). VerilogA can be used for implementation of behavioural models of physically complex electronic components like ESD protection devices with snapback, which are often based on the combination of advanced technologies of diodes, transistors or SCRs.

The quasi-static behaviour is modelled by definition of groups of I and V variables for inflection points in the IV curve. These variables are placed to define boundaries of device working regimes like the Vt1, It1-trigger point of the snapback device and in between to improve accuracy of the model.

The calibration of the model can be easily achieved by tuning these variables. The transition from one inflection point to the other one will be described by linear or non-linear functions defined in the verilogA code. Figure 111 shows the general idea, how the I-V curve can be subdivided and modelled with a set of I-V variables using VerilogA.

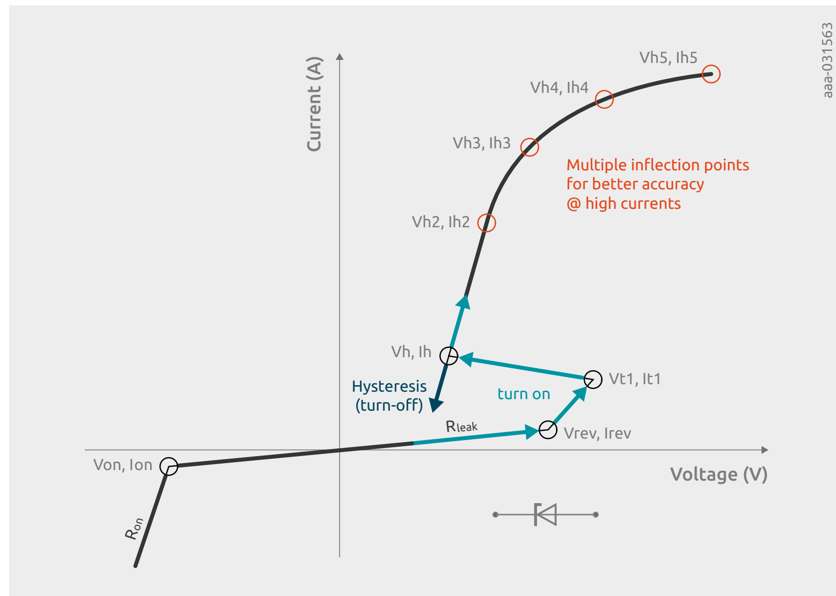


Figure 111 | The model of the quasi-static I-V curve of unidirectional ESD protection device with snapback showing variable groups placed into inflection points responsible for tuning of model working regimes

Additionally, hysteresis behaviour, which comes in play during turn-off of the device, needs to be implemented in the model. In that case, the model will follow another IV curve definition. The unphysical overshoot which may happen by transition according to the initial IV curve will be prevented. Figure 112 shows this difference.

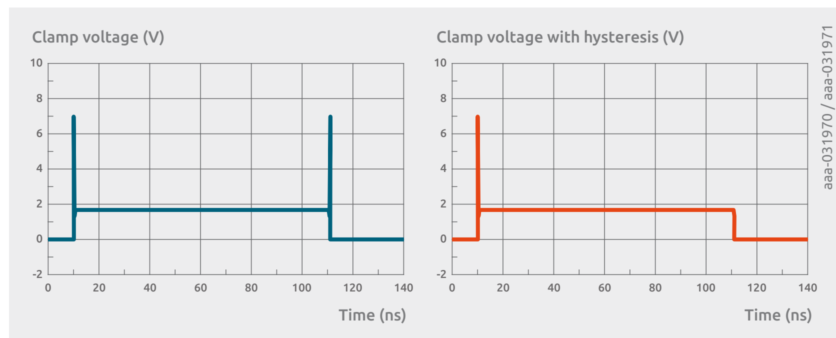


Figure 112 | The graphic on the left illustrates the unphysical voltage overshoot during turn-off of the snapback ESD protection device. In the right graphic this peak is compensated by implementation of hysteresis behaviour

Another advantage of the VerilogA model is that it can also be embedded inside other simulation programs like ADS and used for transient system-level analysis. The model itself can be further extended by adding other discrete components to it. The addition of inductance will change the pure quasi-static model to semi-dynamic, although only partly reflecting the inductive voltage overshoot of the modelled device, since the snapback delay is not implemented here.

Therefore in order to capture all dynamic effects properly, a full dynamic models are needed. This also eliminates some convergence problems related to abrupt slope change during snapback in VerilogA and consequently enables more precise analysis of fast transient ESD events before steady state.

Implementation example:
bidirectional ESD Protection device with snapback

```
//******************************************************************
// SEED Quasi-static transient model of
// ESD protection device with snapback: PESD3V3Z1BSF
//
// Model working regions: leakage, snapback, linear and non-linear (self-heating)
// Additional effects: Hysteresis behaviour by turn-off of the device
//
// For further questions please contact:
// Sergej Bub
// System Level ESD Expert
// sergej.bub@nexperia.com
// Nexperia Germany GmbH
//******************************************************************
//*
`include "constants.vams"
`include "disciplines.vams"
//*
//******************************************************************
module PESD3V3Z1BSF_QSTM_M1(cathode, anode);
  inout cathode;
  electrical cathode;
  inout anode;
  electrical anode;
  parameter real Ron=0 from [0:inf);
  parameter real Von=0.8 from [0:inf);
  parameter real Vrev=6.3 from [0:inf);
  parameter real Rleak=1M from (0:inf);
  parameter real Vt1=8.22 from (0:inf);
  parameter real It1=0.13 from (0:inf);
  parameter real Vh=1.78 from (0:inf);
  parameter real Ih=0.272 from (0:inf);
  parameter real Vh2=4.8 from (0:inf);
  parameter real Ih2=22 from (0:inf);
  parameter real Vh3=11 from (0:inf);
  parameter real Ih3=30 from (0:inf);
  parameter real Vh4=55 from (0:inf);
```

```
  parameter real Ih4=35 from (0:inf);
  parameter real Vh5=727 from (0:inf);
  real Ion;
  real Irev;
  real Rdyn;
  real vout;
  real Iin;
  integer state;
  analog begin
    @(initial_step) begin
      state = 1;
      Ion = -Von/Rleak;
      Irev = Vrev/Rleak;
      Rdyn = Vh2/Ih2;
    end
    Iin = I(anode,cathode);
    @(cross(Iin-Irev,1)) state=1;
    @(cross(Iin-Ih,-1)) state=-1;
    vout = -Von+(Iin-Ion)*Ron;
    if (Iin>Ion) vout = Iin*Rleak;
    if (state>0) begin
      if (Iin>Irev) vout = Vrev + (Iin-Irev)*(Vt1-Vrev)/(It1-Irev);
      if (Iin>It1) vout = Vt1 + (Iin-It1)*(Vh-Vt1)/(Ih-It1);
      if (Iin>Ih) vout = Vh + (Iin-Ih)*Rdyn;
      if (Iin>Ih2) vout = Vh + (Iin-Ih)*Rdyn + (Iin-Ih2)*(Vh3/
      Ih2)*(1-limexp((Ih2-Iin)/Ih2));
      if (Iin>Ih3) vout = Vh + (Iin-Ih)*Rdyn + (Iin-Ih2)*(Vh3/
      Ih2)*(1-limexp((Ih2-Iin)/Ih2)) +
      (Iin-Ih3)*(Vh4/Ih3)*(1-limexp((Ih3-Iin)/Ih3));
      if (Iin>Ih4) vout = Vh + (Iin-Ih)*Rdyn + (Iin-Ih2)*(Vh3/
      Ih2)*(1-limexp((Ih2-Iin)/Ih2)) +
      (Iin-Ih3)*(Vh4/Ih3)*(1-limexp((Ih3-Iin)/Ih3)) +
      (Iin-Ih4)*(Vh5/Ih4)*(1-limexp((Ih4-Iin)/Ih4));
    end
    if (state<0) begin
      if (Iin>Irev) vout = Vh + (Iin-Ih)*Rdyn;
    end
    V(anode,cathode) <+ vout;
  end
endmodule
//********************************************************************
module PESD3V3Z1BSF_QSTM_M2(cathode, anode);
Here, the same code from module “PESD3V3Z1BSF_QSTM_M1” is used. To
describe the asymmetrical I-V curve of the bidirectional ESD
protection device with snapback, different values should be assigned
to the parameters of the module M2. For symmetrical case, all
parameter values should be kept in module M1.
endmodule
//********************************************************************
```


11.2.2 Dynamic model for ESD protection device with snapback

The goal of behavioural dynamic models is to extend quasi-static models with dynamic characteristics of a given ESD protection device to do full system-level transient analysis for SEED. That means component reaction on the injected ESD pulse needs to be analyzed during two different time frames. The first reflects the impact of current to time ratio (dI/dt) of the rising edge of injected ESD pulse on the device behaviour reflecting its behaviour during the first few nanoseconds. The second is related to its steady state condition, reflecting the window between 70 and 90 ns. The working regimes and effects, as well as implementation approach of the dynamic model for ESD protection device with snapback, are discussed below.

At first, the quasi-static behaviour is considered, and Figure 113 shows the typical I-V curve of the ESD protection device with snapback with four related working regions.

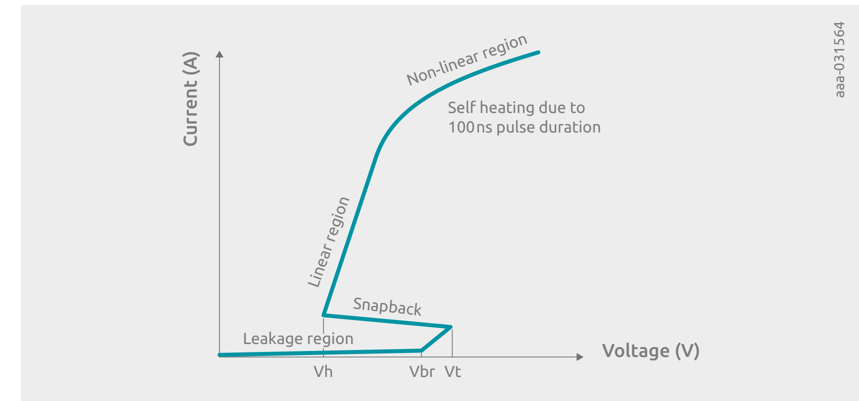


Figure 113 | The quasi-static I-V curve of the ESD protection device with snapback with four working regions: leakage, snapback, linear and non-linear

The first region is the leakage region. Here, the device behaviour can be approximated by small-signal device characteristics using SPICE based models. However, as the signal integrity is not directly in focus of the transient ESD analysis, simple approximation of leakage current by adding of resistor and definition of breakdown voltage by Vbr should be sufficient. The second region is snapback. Here the triggering voltage point is defined by Vt, at which the snapback to holding voltage Vh occurs. The third region is the linear region. This regime is defined by a constant resistance value. Finally the last region is the non-linear region. Due to self-heating of the device a bending of the I-V curve can be observed. To express this behaviour additional resistance will be added. The quasi-static I-V curve, which is needed for model tuning, is obtained by TLP. In that case, averaged values of voltage and current in time window from 70 ns to 90 ns time will be taken.

Figure 114 shows an example of the implementation of the dynamic model in ADS based on the work described in [43].

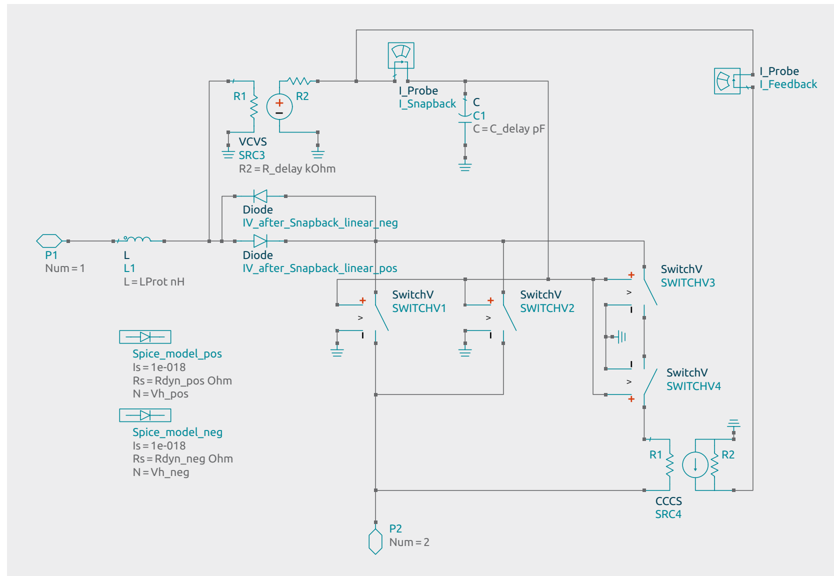


Figure 114 | The dynamic model circuitry of the ESD protection device with snapback implemented in ADS for SEED including full quasi-static and dynamic working regimes without snapback delay

In this model, the leakage and linear regions of the device are defined by SPICE model parameters. The snapback and non-linear regions are implemented with the help of voltage controlled switches. Each switch represents resistance change that is dependent on voltage. Voltage controlled voltage source (VCVS) together with resistor and capacitor belong to a control unit used here for control of these switches. A current feedback loop, which is realized using current controlled current source (CCCS), is an essential part of the model for the realization of the snapback behaviour, as it can keep all switches in pre-defined positions by feeding the current back into the control unit even after the triggering voltage point of the device is reached and the VCVS is no longer able to transfer the initial voltage level to the capacitor of the control unit.

Figure 115 demonstrates an example of current flow after the snapback is occurred and the model is already operating in the linear region. The orange arrows in the picture indicate how the current is flowing during that time.

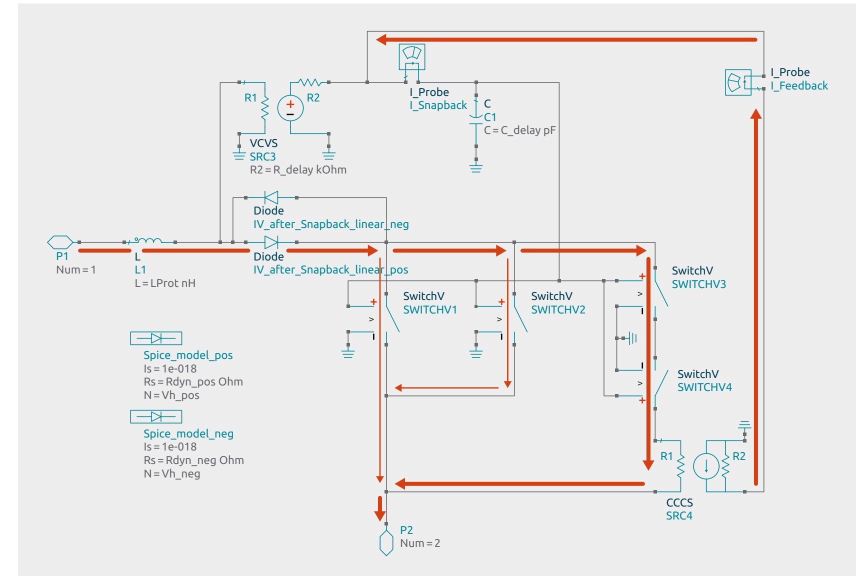


Figure 115 | The current flow in the dynamic model for ESD protection device with snapback without snapback delay, in the linear working regime for steady state condition

Next the dynamic behaviour is considered. Figure 116 shows the typical Imax-Vmax curve, which is generated from the max. values of the TLP measurement of the ESD protection device with snapback including two effects which are responsible for voltage overshoot on the device: inductance (LProt) and conductivity modulation (CM) [14].

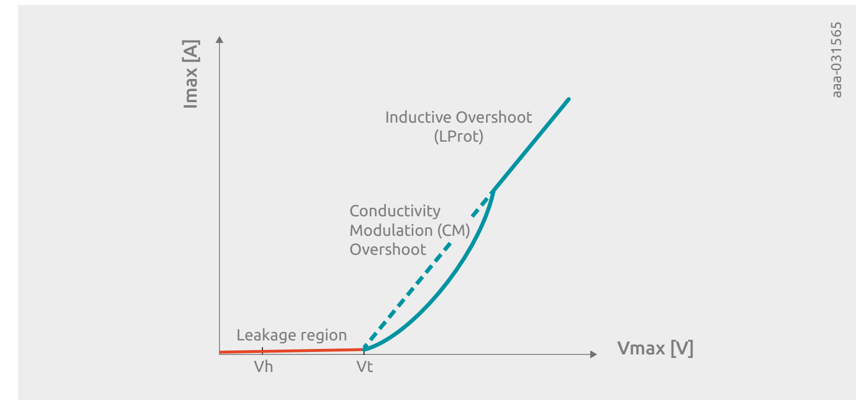


Figure 116 | The dynamic I-V curve of the ESD protection device with snapback with two effects: Inductive Overshoot (LProt) and Conductivity Modulation (CM) Overshoot

The first effect is related to the parasitic inductance of the device. This parasitic inductance can be easily implemented in the model with the help of a lumped element. In that case, the inductive overshoot is modelled according to LProt *dI/dt. The value for LProt can be estimated from vfTLP data or measured with a network analyzer. The obtained value for LProt is usually different from the parasitic inductance considered for signal integrity.

The second effect describes the conductivity modulation of the device which is related to its turn-on behaviour. Depending on the technology used this effect can appear more or less strong, effecting the total voltage overshoot. To model the device resistance change during its turn-on behaviour, an RC network is used, see R (parameter of VCVS) and C capacitor of switch control unit in Figure 114. Depending on the dI/dt of the injected ESD pulse and of the RC value, the overshoot of the ESD protection device can be modelled.

Figure 117 shows an example of dynamic transient simulation of both inductive and CM voltage overshoots. Here each curve represents model reaction on TLP pulse with different current amplitudes but constant rise time.

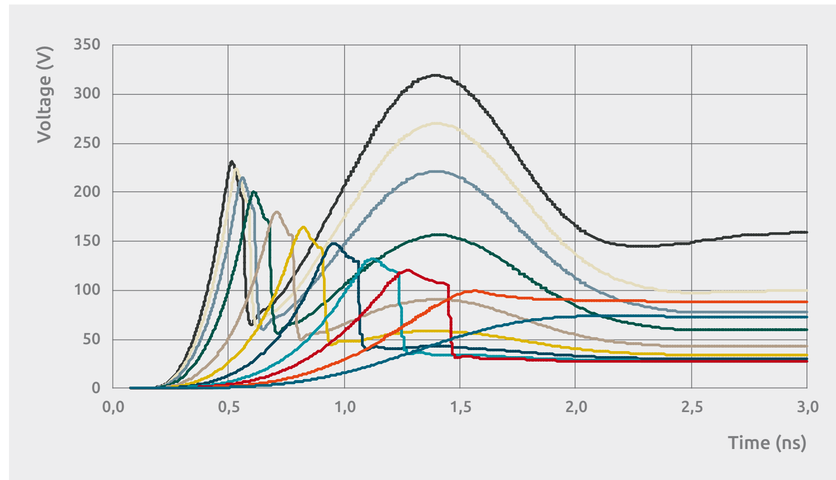


Figure 117 | The time domain curves of the inductive and conductivity modulation voltage overshoots modelled with dynamic modelling approach without snapback delay by application of TLP with different current amplitudes by constant rise time

Although this model can replicate the dynamic behaviour relatively well, one additional effect should be considered and included into the model implementation. This effect is related to the delay of transition from voltage in triggering point before snapback to voltage level after snapback according to applied current level of ESD pulse. In the model, snapback delay prevents the abrupt voltage decrease after the CM peak is reached. Here, the current already starts to flow through the device by keeping the voltage across the device at about triggering voltage and slowly decreasing it. Only in that case a correct modelling of both CM and inductive overshoots can be done simultaneously. Figure 118 shows simulation results of both inductive and CM voltage overshoots after the snapback delay was added into the model circuitry.

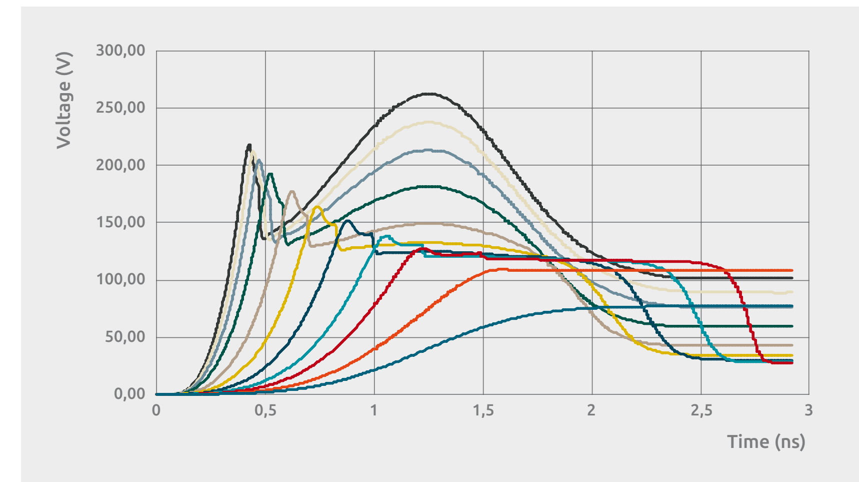


Figure 118 | The time domain curves of the inductive and conductivity modulation voltage overshoots modelled with dynamic modelling approach using snapback delay by application of TLP with different current amplitudes by constant rise time

This is realized using additional CCCS with current loop and another switch, which define the charging speed of the capacitor C of the switch control unit, and delaying the full current transition over the current feedback loop. Figure 119 shows the complete version of the model.

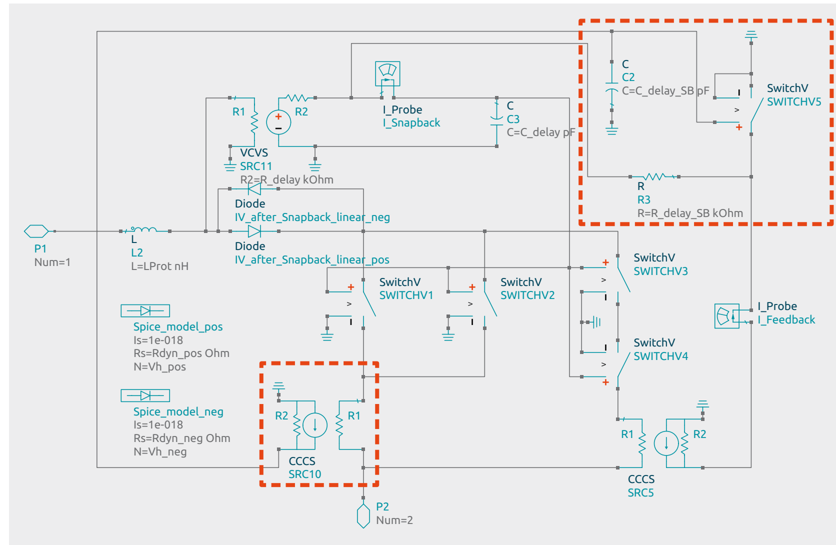


Figure 119 | The dynamic model circuitry, including snapback delay part, of the ESD protection device with snapback implemented in ADS for SEED including full quasi-static and dynamic working regimes

Last but not least, this model can be used in a bidirectional setup. Representing the behaviour of a bidirectional ESD protection device with snapback, where both directions can be tuned separately using dedicated set of variables. This behaviour is realized by programming of the VCVS and CCCS blocks as well as of the switches depending on the sign of the entering ESD pulse amplitude. The opposite or "negative" linear region is defined by addition of second diode SPICE model which is connected reverse-parallel to the diode SPICE model, which is dedicated for "positive" direction of current flow. Thereby two modes of model operation will be covered by this dynamic model, for positive and negative ESD pulses. A change of the model operation mode is controlled by model variable Vpulse, which value can be assigned during simulation: ">0" for positive and "<0" for negative ESD pulses. For proper model operation the Pin1 (P1) of the model should however always be used as a signal pin and Pin2 (P2) should be connected to GND.

11.3 Common-mode choke (CMC) model

The common-mode choke (CMC) is primarily used in a system to suppress the common mode noise of the entering signal. However, its sometimes hidden advantage manifests itself in suppression of ESD pulses, which can impair the system performance and lead to system upsets or even its degradation. Since usage of a CMC alone is typically not enough to guarantee a high level of system ESD robustness, a combination with an ESD protection device will be often suggested. This symbiosis can sufficiently improve the final ESD robustness of the system.

Typically, S-Parameters will be obtained to characterize and model the CMC behaviour. The problem arises however when a CMC with ferrite core is used. In that case effects like saturation start to play an important role, since the current flow through it cannot be suppressed any longer. To include this effect and also to capture its dynamic characteristic, reflected as current overshoot due to turn-on of the CMC, an appropriate model beyond small-signal range is needed. Figure 120 demonstrates modelling results of the extended CMC model, which is based on the adapted dynamic modelling approach described in Section 11.2.2 including S-Parameters of the CMC.

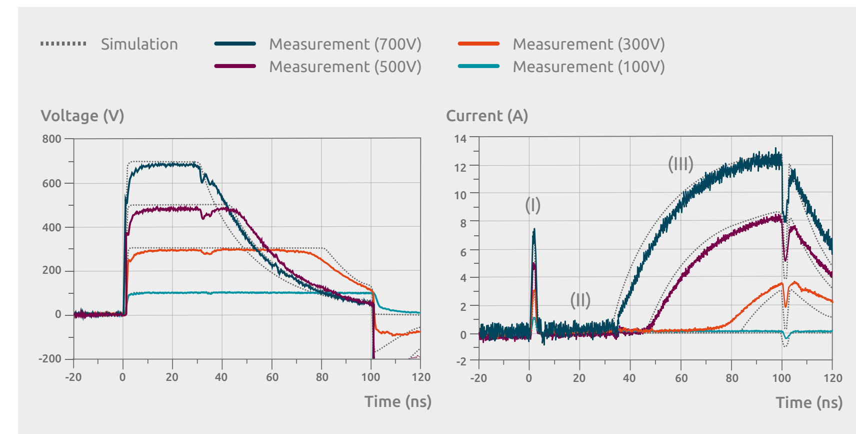


Figure 120 | The simulation results of the CMC model compared with measurements representing both dynamic (I) and quasi-static: small-signal (II) and saturation (III) working regions

The evaluation of voltage and current curves in time domain identify two working regimes: dynamic and quasi-static. The dynamic behaviour of the CMC is reflected by rising edge of voltage and corresponding current peaks (I). Here the CMC works as an inductor. The quasi-static behaviour of the CMC can be subdivided into two further regions: small-signal (II), where the CMC transforms the open condition of second coil preventing the current flow through the first coil and keeping the voltage at the constant level, and saturation region (III), a moment where the energy cannot be stored any longer inside the CMC and it starts to change it's characteristic to a resistance, whereby the current starts to flow and voltage drops dramatically.

11.4 ESD generator model

For transient analysis of modelled system behaviour during an ESD event, an ESD Pulse model is required. An ESD generator is used to replicate ESD events, which can occur in the field. Therefore, for accurate evaluation of system-level behaviour an ESD Generator model will be used in SEED. Figure 121 illustrates an example of how the ESD generator model can be implemented in the form of an equivalent circuit. This model is based on the modelling solutions proposed and discussed for ESD generators in [43–45].

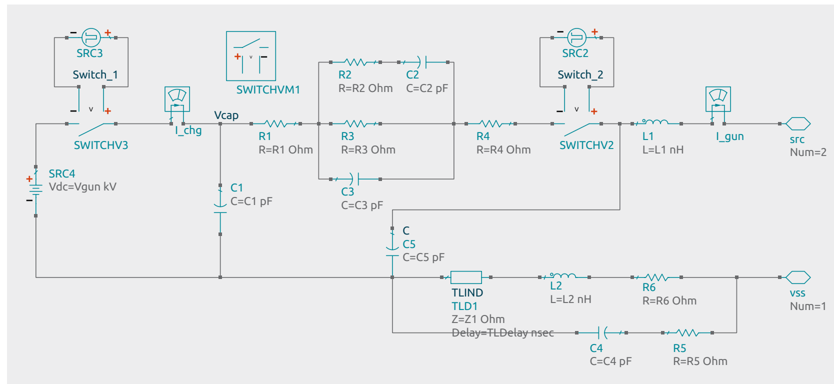


Figure 121 | The equivalent circuit based model of an ESD generator implemented in ADS

Before this model can be used as a stimulus for a system-level transient analysis it should be first tuned to the calibration measurement results of the used ESD generator. Figure 122 shows the comparison of simulated and measured time domain current curve. The measured curve was obtained according to the setup defined in the IEC61000-2-4 standard, whereas an injection of 1 kV ESD pulse was done into a 2 Ω Pellegrini target.

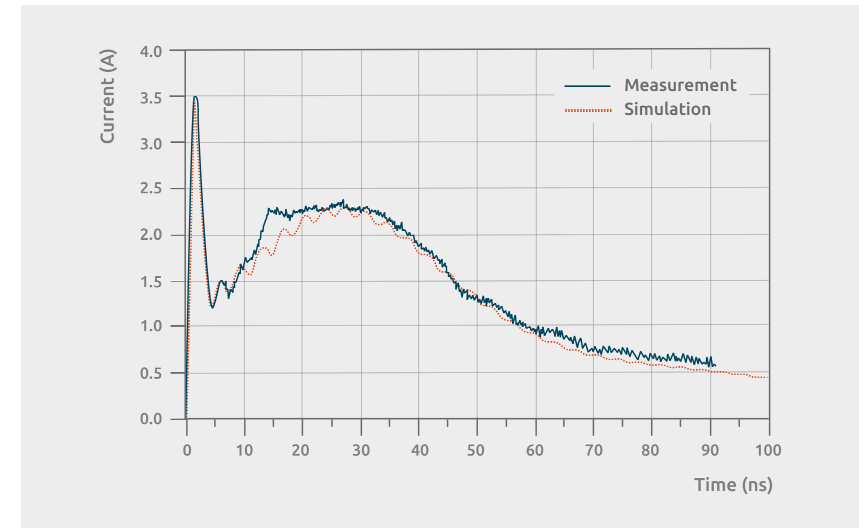


Figure 122 | The simulation result of ESD generator model tuned on time domain current curve obtained by calibration of ESD generator acc. IEC61000-4-2 standard

11.5 Simulation example 100BASE-T1

The OPEN Alliance has specified an ESD protection network for 100BASE-T1 and defined procedures to test compliance of external ESD protection devices, see Section 7.4. According to this specification the ESD protection device is placed in front of the CMC. This helps trigger ESD protection devices earlier, due to the CMC, but also protect passive components located on the signal trace against ESD. Moreover, due to the external ESD protection device position the need to adapt its characteristic on IC requirements vanishes. This makes the initial choice as well as later exchange of ESD protection components or ICs, more flexible and independent from each other.

To anticipate the ESD Robustness of the system the *ESD Discharge Current Test* is defined [32]. This test determines the rest current which flows into the system IC during an ESD event and helps to identify whether the ESD protection device used for protection of 100BASE-T1 transceiver can guarantee a certain level of ESD robustness. For that purpose, an ESD Gun test is performed using the test board shown in Figure 123.

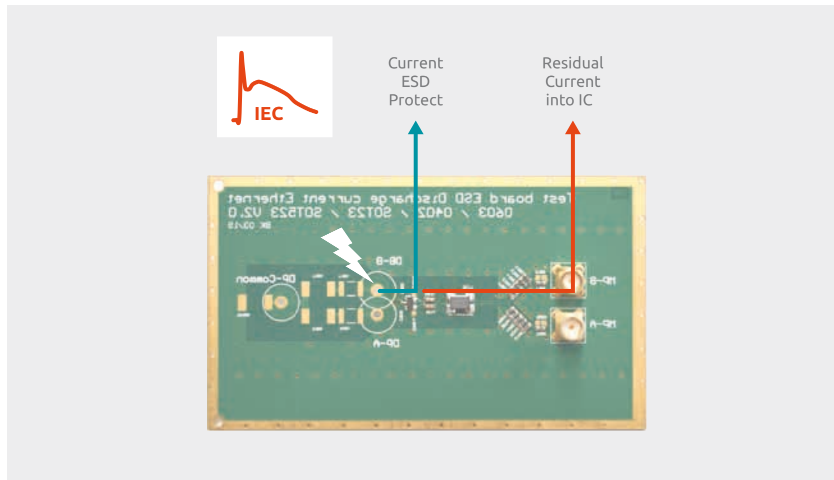


Figure 123 | The IEC pulse of an ESD generator is injected into the external pin of the depicted test board leading to current spread between the external ESD protection device and the IC, where the residual current flow into the IC can be evaluated

The following section will show how SEED methodology can be applied to model this test procedure to predict on simulation level the current flow into the IC during ESD event and to draw conclusions about the ESD robustness level of the overall system including ESD protection of its passive components. Here the general steps will be treated, for more detailed information please refer to the paper "Efficient prediction of ESD discharge current according to OPEN Alliance 100BASE-T1 Specification using SEED" [40], which can be found on Nexperia's website.

To perform transient simulation of 100BASE-T1 ESD protection network, each part of the system should be modelled first. Figure 124 gives an overview over the equivalent circuit block diagram of SEED model of the ESD Discharge Current Measurement reference circuit according to OPEN Alliance Specification resembling the PCB shown in Figure 123.

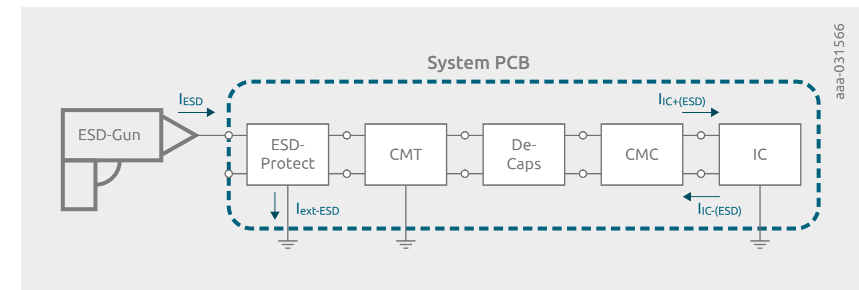


Figure 124 | The equivalent circuit block diagram of SEED model of the ESD Discharge Current Measurement reference circuit according to OPEN Alliance specification

Each block depicted here, represents a model optimized for SEED. All shown models can be grouped together to three model types: equivalent circuit based model (ESD Gun), models which can be implemented in form of a network with lumped elements (CMT, De-Caps and IC) and behavioural model (ESD protection device, CMC).

To protect the system against ESD, the PESD2ETH1G-T ESD protection component was chosen. One of the challenges here was to ensure that the used ESD protection device triggers before the CMC goes into saturation mode, where the current flow into the IC rapidly increases and may damage the system. To ensure that, a safety margin of about 50% between triggering point of the ESD component and onset of saturation of the CMC was kept by choosing appropriate combination of ESD protection and CMC components. Figure 125 visualizes the CMC I-V curve including the triggering point Vt_ext_ESD of used ESD protection device.

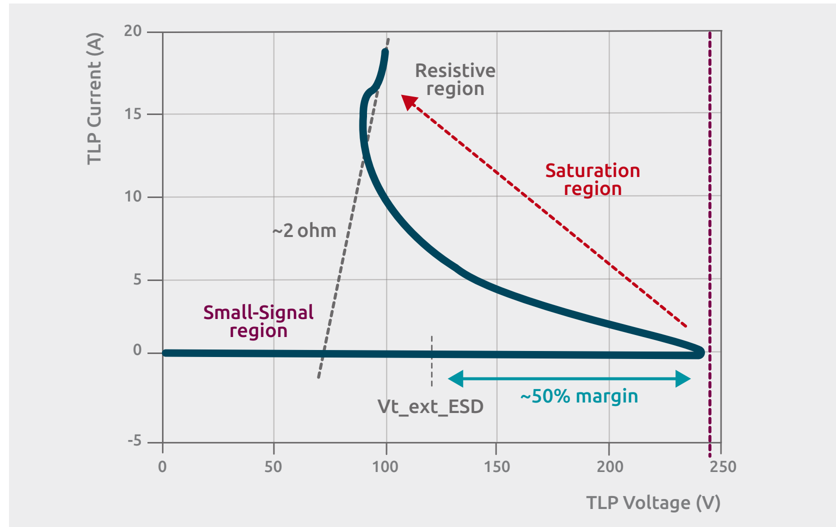


Figure 125 | The I-V curve of the CMC obtained by TLP shows small-signal, saturation and resistive working regions. The Vt_ext_ESD voltage triggering point of the external ESD protection device indicates ca. 50% safety margin to the onset point of saturation of used CMC component.

The corresponding simulation results of quasi-static and dynamic behaviour of the PESD2ETH1G-T ESD protection device, which dynamic model was already discussed earlier in this chapter and is depicted in Figure 120, can be observed in Figure 126.

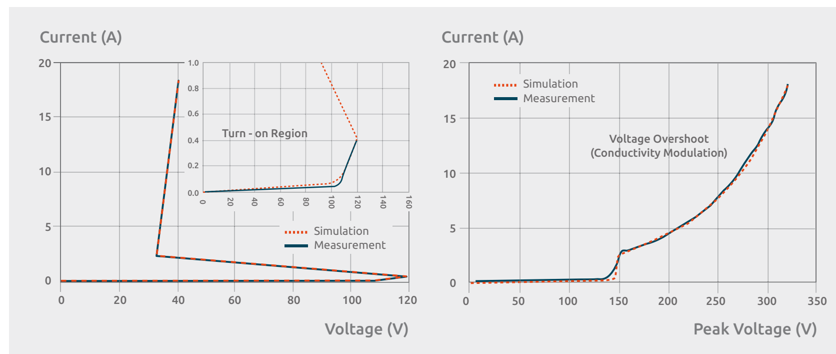


Figure 126 | The left graphic shows the simulation result of the quasi-static I-V curve of the PESD2ETH1G-T ESD protection device including zoom-in of its turn-on region, the right graphic gives an overview over its dynamic characteristic described with I-Vmax curve

Finally, the residual current flow into the IC will be evaluated. For that purpose, the full SEED model depicted in Figure 124 will be used. In Figure 127 the comparison of simulated versus measured rest current flow into the IC is shown. Here, a positive ESD Generator discharge of 4 kV into the external system pin was applied and evaluated.

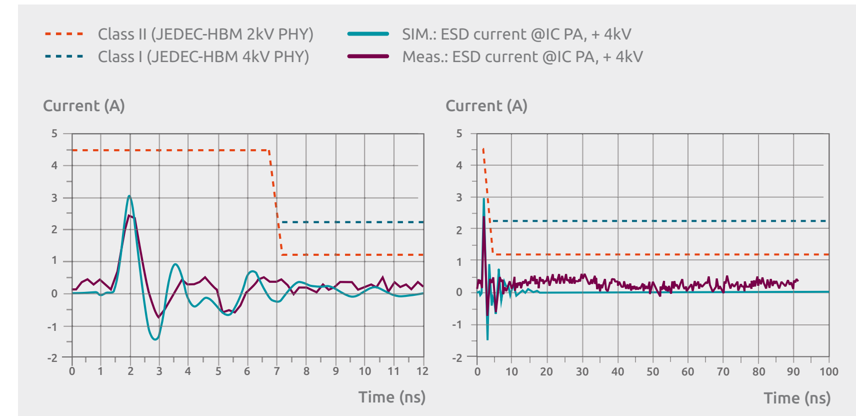


Figure 127 | The resulting time domain curves of measured vs. simulated residual current into the IC with focus on dynamic (left graphic) and quasi-static (right graphic) behaviour

Both graphics demonstrate the resulting simulated current curves in time domain concurrently showing the measured current at the IC I/O pin. The yellow and red dashed lines show the limits of the I and II Class of the JEDEC-HBM standard [15] accordingly. The used SEED model provides an estimation of the tested system predicting ca. 20% higher maximal current peak. For the static part of the curve however, the simulation rather underestimates the measurement.

The observed deviations between the simulated and measured results can be explained by electromagnetic coupling effects, which are not encountered in the actual SEED model, i.e. effects related to crosstalk or electromagnetic radiation of ESD generator relay. In such case, the maximal current measured at the IC I/O pin(s) may be destructively attenuated by virtue of coupling effects between the ESD gun and the test board components like board traces, CMT network or CMC.

To minimize these effects an additional effort could be spent to improve the shielding of the board from the direct impact of the relay as here the ESD generator has not been shielded against the DUT. Also, to improve the modelled behaviour of the system an S-Parameters model of the PCB may be added to the SEED model.

Despite these deviations, the proposed SEED model has proven to be a good solution for estimation of the overall system transient response under ESD conditions. Furthermore, it can be used for the prediction of the system-level ESD robustness according to IEC61000-4-2 [6] and evaluation of the IC robustness according to JEDEC-HBM [15] requirements. It can also be useful in studying the impact of variation of system and external ESD protection device parameters to achieve the optimal protection of the system IC in order to minimize the engineering and verification time.

Chapter 12
Summary

Increasing data rates, connectivity, and ADAS are pushing automotive interfaces to regions formally dominated by the mobile and computing industry. The technical challenge is to implement these systems while maintaining the high requirements for EMC and especially ESD of the automotive industry. Todays and tomorrows challenges differ from traditional approaches of ESD protection. As for classic interfaces, an ESD protection device could be just taken from the shelf and somehow helped, modern interfaces requires more system knowledge and understanding of the ESD protection device itself to select the right device and increase system level robustness.

This handbook introduced the foundation of both characteristics of ESD protection devices and system level and device characterization test to understand how the device behaves in desired system operation and during an ESD event. The following chapters focused on the physical layer properties of different interfaces, how ESD protection devices are selected, and possible compliance requirements. The final chapter introduces the fundamentals of SEED and showed an example for an automotive interface.

As various examples in the Handbook showed, there is no one fits all solution and this Handbook is meant to provide guidance in finding the optimal choice. Nexperia provides a wide portfolio of products for all discussed interfaces and applications and is permanently developing new cutting-edge technology products optimizing the three pillars of ESD protection: robustness, signal integrity, and system protection. For questions and suggestions do not hesitate to contact us.

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Abbreviations

- ADAS — Advanced driver assistance systems
- ADC — Analog/digital converter
- AOI — Automated optical inspection
- APIX — Automotive Pixel Link

- CAN — Controller Area Network
- CCCS — Current controlled current source
- CCW — Counterclockwise
- C_d — Diode capacitance
- CEC — Consumer electronics control
- CM — Conductivity modulation
- CMC — Common-mode choke
- CMT — common-mode termination
- C_t — Tip capacitance
- CW — Continuous wave / clockwise

- DC — Direct current
- DDC — Display data channel
- DFP — Downstream forcing port
- DPI — Direct power injection
- DUT — Device under test
- DVD — Digital versatile disk

- ECU — Electric control unit
- EDID — Extended display identification data
- EFT — Electrical fast transients
- EMC — Electromagnetic compatibility
- EMI — Electromagnetic interference
- EOP — End-of-packet
- EOS — Electrical overstress
- ESD — Electrostatic discharge

- f_{-3dB} — Frequency with -3dB attenuation, loss
- FET — Field-effect transistor
- FPD-link — Flat Panel Display Link

- GND — Ground
- GPS — Global Positioning System
- GSM — Global System for Mobile Communication

- HBM — Human Body Model
- HDCP — High-bandwidth Digital Content Protection
- HDMI — High Definition Multimedia Interface
- HMM — Human Metal Model
- HS — High speed

- IC — Integrated circuit
- I_{hold} — Hold current
- IoT — Internet of Things
- I_{PP} — Peak pulse current
- I_{PPM} — Peak pulse current maximum, single pulse
- I_{RM} — Leakage current at VRWM
- IVN — In-vehicle network

- LIN — Local Interface Network
- LS — Low speed
- LVDS — Low-voltage differential signal

- MC — Mode conversion
- MDI — Media dependent interface
- MIPI — Mobile Industry Processor Interface
- MOSFET — Metal oxide field-effect transistor

- NFC — Near field communication
- NRZ — Non return to zero (code)
- NRZI — Non return to zero inverted (code)

- PCB — Printed circuit board
- PD — Power delivery
- PLL — Phase-locked loop
- PoA — Power-over-APIX
- PoC — Power-over-Coax
- PoDL — Power-over-Data-line
- PoE — Power-over-Ethernet
- P_{pp} — Peak pulse power

- RD — Running disparity
- R_{dyn} — Dynamic resistance
- RF — Radio frequency
- RX — Receiver input

- S_{11} — Return loss
- S_{21} — Insertion loss
- SBC — System basis chip
- SBU — Sideband usage
- SCR — Silicon controlled rectifier
- SEED — System Efficient ESD Design
- SerDes — Serializer/Deserializer
- SoC — System-on-Chip
- S-parameters — Scattering parameters
- STP — shielded twisted-pair
- SWCAN — Single-wire CAN

- T_{amb} — Ambient temperature
- T-Box — Telematic box
- TDR — Time Domain Reflection
- T_j — Junction temperature
- TLP — Transmission-line pulse
- TMDS — Transmission minimized differential signaling
- TPA — Test point adapter
- T_{stg} — Storage temperature
- TTL — Transistor-transistor logic
- TVS — Transient voltage suppressor
- TX — Transmitter output

- UFP — Upstream forcing port
- USB — Universal Serial Bus
- UTP — Unshielded twisted-pair

- V2X — Vehicle to anything
- V_{BR} — Breakdown voltage
- V_{CL} — Clamping voltage
- VCVS — Voltage controlled voltage source
- VDM — Vendor defined massages
- V_{ESD} — Maximum ESD voltage, robustness
- V_F — Forward voltage
- VF-TLP — Very fast TLP
- V_{hold} — Hold voltage
- VPN — Virtual private network
- V_{RWM} — Stand-off voltage, max. operation voltage

- WiFi — Wireless local area network (artificial abbreviation)

- XOR — Exclusive OR, logical function

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ESD Application Handbook — Automotive Edition
Protection concepts, testing and simulation for modern interfaces
Design Engineer's Guide

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July 2020

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ISBN 978-0-9934854-5-9

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